The Operational Domain Explorer: A Comprehensive Framework to Unveil the Thermal Landscape of Silicon Dangling Bond Logic Beyond Conventional Operability

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***Abstract*— As *Silicon Dangling Bond* (SiDB) logic emerges as a promising beyond-CMOS computing paradigm, evaluating its robustness against fabrication imperfections and thermal noise becomes crucial. The *Operational Domain* framework provides a foundation for such assessments but overlooks key *Figures of Merit* (FoMs) such as temperature robustness, alternative input paradigms, and I/O integrity validation. This paper introduces new methodologies that extend operational domains to incorporate these factors, enabling a more comprehensive analysis of SiDB gate stability. Implemented in the open-source *Operational Domain Explorer*, these methods provide high-resolution robustness evaluations. Our results reveal that critical temperature domains exhibit highly uneven structures, previously thermally unstable gates can function at room temperature under specific material parameters, and enforcing I/O integrity significantly reduces temperature stability. By addressing these overlooked aspects, this work refines SiDB robustness evaluation and provides new insights into optimizing both simulation methodologies and fabrication strategies for more reliable SiDB-based computing architectures.**

I. Introduction

As the miniaturization of transistor technologies faces increasing challenges, the search for alternative platforms that offer higher integration density and lower power consumption has intensified. *Silicon Dangling Bonds* (SiDBs) have emerged as a promising candidate, with experimental demonstrations of functional logic devices at nanoscale dimensions [1]–[3]. Companies like *Quantum Silicon Inc.* are already investing heavily in SiDB research, highlighting its potential to revolutionize nanoscale computing [3]–[5].

The advent of SiDB technology has sparked significant research interest, leading to the development of design automation tools and physical simulators to support SiDB-based computational devices [6]–[9]. However, SiDBs' reliance on atomically precise fabrication renders them susceptible to fabrication errors, environmental defects, and material inhomogeneities, all of which can disrupt logic operation. To address these challenges, the concept of the *Operational Domain* was introduced to evaluate the resilience of SiDB logic against variations in physical parameters before fabrication [6], [10], [11].

While the operational domain provides valuable insights into the stability of SiDB logic, it primarily focuses on a single metric: *operability*. This limitation overlooks the interplay between physical parameters and various *Figures of Merit* (FoMs), such as temperature robustness, which is crucial for nanoscale technologies [12]. Although SiDBs can, in principle, operate at room temperature, the actual thermal stability of individual gate layouts varies significantly [12]. Additionally, kink states regularly occur in wire segments that see individual input bits flipped. However, these logic errors are sometimes masked when gate operation prevails in isolation. Since operational domain simulations are computationally costly, it is often infeasible to investigate more than one gate at a time, meaning these effects remain underexplored. Previous analyses also neglected the effect of perturber placement for input signal encoding, which plays a critical role in the reliability and reproducibility of operational domain data.

SiQAD, the primary CAD tool for SiDBs [6], enables design and simulation but lacks dedicated robustness analysis capabilities. As a result, researchers must manually approximate resilience by running individual simulations across numerous parameter settings—an infeasible task due to the sheer number of required evaluations, which frequently exceed tens of thousands. Moreover, domain-specific expertise is necessary to interpret the results and extract meaningful insights, limiting non-experts from gaining valuable knowledge on SiDB logic robustness.

This paper addresses these gaps by introducing the *Critical Temperature Domain* that extends the concept of operational domains to incorporate thermal robustness. Furthermore, the effects of perturber placements for input signal encoding and I/O pin integrity are considered to obtain more reliable and reproducible robustness data. The proposed methodology is made accessible via an open-source GUI tool, the *Operational Domain Explorer*. To mitigate the consequently rising computational cost of the proposed methods, the tool integrates high-performance physical simulation engines and efficient algorithms for domain reconstruction. The resulting real-time robustness analyses fill a critical gap in SiDB design methodologies.

Applying the proposed tool, we reveal several critical findings about the thermal stability of SiDB logic gates:

1) Nearly all critical temperature domains exhibit a highly uneven and rugged structure. This challenges previous assumptions that SiDB gates fail at a uniform temperature threshold and highlights the necessity of incorporating thermal resilience into gate design methodologies.
2) Some gates previously thought thermally unstable can maintain functionality above room temperature. This insight was previously masked when evaluating gates solely at default material parameters, where these structures appeared far less resilient. These findings suggest that manufacturing processes could be optimized to target material parameter regions that maximize gate resilience.
3) A substantial reduction in temperature robustness is observed across most layouts when strict I/O validation is applied. This underscores the necessity of rigorous validation in SiDB circuit evaluation to ensure that robustness assessments reflect genuine operational limits rather than favorable but misleading internal states.

By highlighting these critical insights, this paper paves the way for holistic analyses of SiDB logic devices, fostering the development of more robust gate designs that are essential for the future success of this technology.

The remainder of this paper is structured as follows: Section II provides background on SiDBs and the operational domain, including an overview of according reconstruction algorithms. Section III details the proposed methodologies and the *Operational Domain Explorer* tool. Section IV presents and discusses the simulation results of a critical temperature domain analysis, and Section V concludes the paper.

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II. Preliminaries

This section establishes the foundational concepts essential for the discussions that follow. Section II-A begins with an overview of the SiDB logic platform, emphasizing its potential as a transformative beyond-CMOS computing technology. Next, Section II-B examines the principles of SiDB physical simulation, with particular attention to the role of material-specific parameters in governing the behavior of SiDB gates. Precisely understanding these influences is crucial, as even minor variations can significantly impact gate functionality. Finally, Section II-C introduces the concept of the operational domain.

A. Silicon Dangling Bond Logic

SiDBs are atomically precise, chemically uniform quantum dots that can be fabricated on n-doped hydrogen-passivated silicon (H-Si(100)-2×1). Their creation relies on the precise removal of individual hydrogen atoms from the silicon surface using an atomically sharp *Scanning Tunneling Microscope* (STM) tip. This process locally breaks the covalent Si-H bond, leaving behind an exposed sp^3-orbital on the silicon lattice, which constitutes an SiDB. The resulting atomic-scale structure is depicted in Fig. 1a as a ball-and-stick side view and in Fig. 1b as a top-down visualization of the crystal lattice. Depending on its electrostatic environment, an SiDB may assume one of three charge states: negatively charged (fully occupied), neutrally charged (half occupied), or positively charged (empty). The precise charge configuration is governed by the local electrostatic potential, which shifts the charge transition levels relative to the Fermi energy E_F.

The unique electrostatic characteristics of SiDBs make them exceptionally well-suited as fundamental building blocks for nanoscale logic devices [1], [13], [14]. A prominent example of SiDB-based computation is illustrated in Fig. 1c, where a binary wire is realized through electrostatic coupling. Within this *Binary-Dot Logic* (BDL) paradigm, electrostatic repulsion between adjacent SiDBs ensures that each pair consists of one neutrally charged and one negatively charged site (marked in green rectangles). This controlled charge distribution propagates binary information along the wire, effectively encoding the logical state `1`.

SiDB logic harnesses the discrete positioning of electrons as the basis for binary information processing. This principle extends naturally to the design of logic gates.

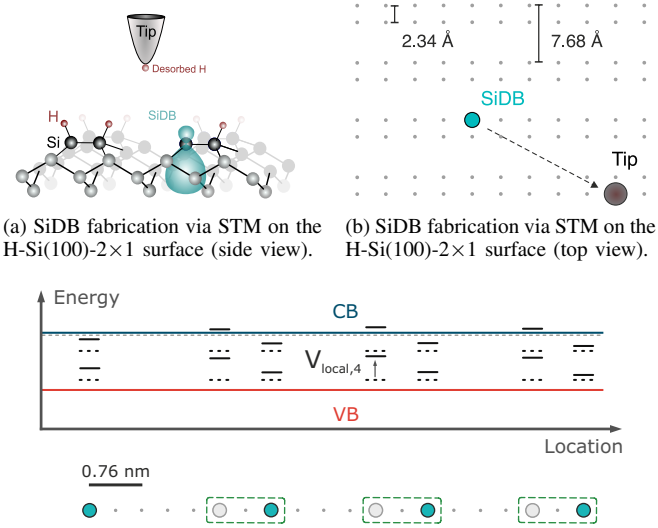
Example 1. *The SiDB layout depicted in Fig. 2a exemplifies a two-input OR gate. When supplied with the binary input* `10` *(as shown), the electrostatic interactions among the SiDBs result in the expected output state of* `1`*, demonstrating the feasibility of SiDB-based logic operations.*

Notably, Huff *et al.* [1] successfully fabricated an eight-SiDB BDL wire and demonstrated an OR gate occupying an area of less than $30\,\mathrm{nm}^2$, showcasing the extreme scalability of this approach.

A defining advantage of SiDB-based logic is the tunability of its charge states, which facilitates the development of highly compact and efficient circuit designs. This adaptability positions SiDB technology as a compelling candidate for beyond-CMOS computation, offering the potential for ultra-dense and low-power computing architectures.

B. Physical Simulation of SiDBs

The precise simulation of SiDB layouts is indispensable for predicting their functional behavior and facilitating design exploration without necessitating costly and time-intensive fabrication. Given the inherently electrostatic nature of SiDB interactions, modeling the electrostatic potential landscape serves as a fundamental approximation for understanding system behavior. In free space and conventional dielectric materials, potential energy between charged entities typically follows an inverse dependence on distance, scaling as $1/d$. However, in the case of SiDBs, an additional exponential attenuation must be considered due to electrostatic screening effects arising from free charge carriers, as experimentally validated by Huff *et al.* [15]. The electrostatic potential $V_{i,j}$ induced at a given site i by an SiDB occupying state $n_j \in \{-1, 0, 1\}$ at position j is expressed as [1], [15]:



(a) SiDB fabrication via STM on the H-Si(100)-2×1 surface (side view).

(b) SiDB fabrication via STM on the H-Si(100)-2×1 surface (top view).

(c) Energy landscape of seven interacting SiDBs.

Fig. 1: The SiDB logic platform.

$$V_{i,j} = -\frac{q_e}{4\pi\epsilon_0\epsilon_r} \cdot \frac{e^{-\frac{d_{i,j}}{\lambda_{tf}}}}{d_{i,j}} \cdot n_j, \tag{1}$$

where q_e, ϵ_0, and ϵ_r denote the elementary charge ($q_e = -e$), vacuum permittivity, and relative permittivity, respectively. The parameter $d_{i,j}$ represents the spatial separation between the two SiDB sites, while λ_{tf} corresponds to the *Thomas-Fermi screening length*, which accounts for screening effects within the material [1]. By leveraging the principle of superposition, the total electrostatic potential energy within an SiDB arrangement is formulated as:

$$E = -\sum_{i<j} V_{i,j} \cdot n_i \cdot q_e. \tag{2}$$

As outlined in Section II-A, the behavior of an SiDB layout is dictated by electrostatic interactions that dynamically shift the charge transition levels of individual SiDBs. Such shifts may result in charge state alterations, for instance, from negative to neutral or from neutral to positive, particularly in the presence of strong local electrostatic influences. Given an SiDB layout containing k SiDBs, the theoretical configuration space encompasses 3^k distinct charge distributions. However, not all of these are *physically valid*, as the system must satisfy two fundamental criteria: *Population Stability* and *Configuration Stability*, as introduced by Ng *et al.* [6]. Only charge distributions that fulfill both conditions can be considered valid.

a) Population Stability: The charge state of any individual SiDB is inherently constrained by its electrostatic environment, which modulates its charge transition levels. The cumulative electrostatic potential experienced at a given SiDB site i due to surrounding SiDBs is formally described by:

$$V_{local,i} = \sum_{j,j\neq i} V_{i,j}. \tag{3}$$

Depending on the magnitude of this local potential, an SiDB may adopt one of the three distinct charge states: negative, neutral, or

positive. The following stability conditions determine the precise charge state of an SiDB i: an SiDB remains negatively charged if $\mu_- + V_{local,i} \cdot q_e < 0$, transitions to a positively charged state if $\mu_+ + V_{local,i} \cdot q_e > 0$, and remains neutral otherwise.

b) Configuration Stability: Beyond individual charge states, the system must also exhibit stability in its overall charge distribution. Configuration Stability mandates that no spontaneous single-electron transfer event should reduce the total electrostatic potential energy of the system. If such an energetically favorable transition were possible, the system would naturally evolve toward that lower-energy configuration.

In a given SiDB layout, multiple *physically valid* charge distributions can exist. As dictated by Equation 2, the total electrostatic potential energy of the system is inherently dependent on the specific charge configuration. At sufficiently low temperatures, the system will tend toward the charge distribution that minimizes its total energy. Consequently, rather than evaluating all possible valid configurations, it suffices to identify the *ground state*—the charge distribution corresponding to the global energy minimum. Determining the ground state constitutes the task of physical simulation [6]–[8], [16].

C. Operational Domains

SiDBs are inherently prone to inhomogeneity in physical systems, which have been shown to disturb gate operation [15]. This circumstance is caused by the dependence of the electrostatic interaction on the material-specific parameters ϵ_r and λ_{tf} as given by Equation 1. Consequently, any changes in these values significantly influence the behavior of a given SiDB gate.

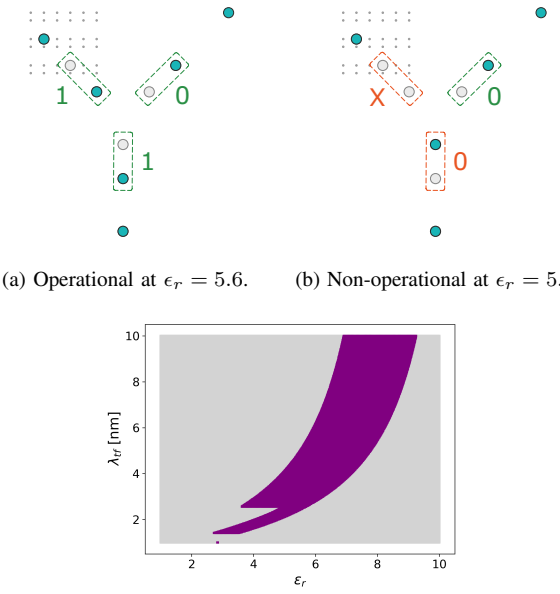
Example 2. *The influence of the* relative permittivity ϵ_r *is illustrated in Fig. 2 at the example of the OR gate from [6] with an input pattern of* `10` *applied. While the SiDB gate computes the correct logic output of* `1` *in Fig. 2a for the standard values* $\lambda_{tf} = 5\,\mathrm{nm}$ *and* $\epsilon_r = 5.6$*, a slight reduction of* ϵ_r *to* 5.5 *leads to a stronger electrostatic interaction, and thus, reduces the charge population of the ground state. Hence, as illustrated in Fig. 2b, this results in the incorrect logic output of* `0`*, rendering the gate non-operational.*

The so-called *Operational Domain* was proposed as a methodology to evaluate the extent of physical parameter variations that an SiDB logic gate is able to tolerate by plotting the logical correctness of that gate's behavior across a predetermined range of physical parameters [6], [11]. Given an SiDB layout L and a Boolean function $f : \mathbb{B}^n \to \mathbb{B}^m$, the operational domain of L in the $(\epsilon_r, \lambda_{tf})$-space given f is defined as the set of coordinate points for which $L \models f$. To determine whether L implements f at any given coordinate point (x, y), this point can be *sampled*, i. e., by conducting 2^n physical simulations—one for each possible input pattern of L—with $\epsilon_r = x, \lambda_{tf} = y$.

Example 3. *An operational domain plot of the OR gate from Fig. 2 can be seen in Fig. 2c, where purple indicates* operational*, i. e., correct gate logic, and gray indicates* non-operational*, i. e., that at least one of the* 2^n *simulations of that sample point yielded incorrect logic behavior.*

Early works applied *grid search* methods to evaluate operational domains [1], [6], but this approach scales poorly due to the quadratic number of sample points required. Each sample point demands multiple physical simulations, with worst-case complexity growing exponentially in the number of SiDBs.

To reduce this complexity, [10] introduced two novel approaches that guide simulation: *flood fill* and *contour tracing*. Flood fill selectively expands the search only within operational regions, reducing simulator calls. Contour tracing exploits the continuous nature of operational domains, focusing on boundary detection to reduce sampling complexity from quadratic to linear. While these advances



(a) Operational at $\epsilon_r = 5.6$. (b) Non-operational at $\epsilon_r = 5.5$.

(c) Operational domain in the $(\epsilon_r, \lambda_{tf})$-space.

Fig. 2: Influence of the relative permittivity ϵ_r on the logic operation of an SiDB OR gate proposed in [6] with input pattern `10` applied, and the gate's resulting operational domain.

enhance scalability, the operational domain remains limited to a binary assessment of gate functionality, overlooking critical *Figures of Merit* (FoMs) such as temperature robustness [12]. Additionally, existing methodologies neglect the influence of I/O pin integrity and input signal encodings, both of which significantly impact reliability. Addressing these shortcomings is essential for a more comprehensive evaluation of SiDB logic robustness.

III. Operational Domain Explorer

To address the shortcomings outlined in the previous section, we introduce the *Operational Domain Explorer*, a novel GUI-based tool that, for the first time, enables high-resolution operational domain reconstruction efficiently and fully automatically while yielding more reliable data. Unlike previous methods requiring manual simulations and domain expertise, our tool integrates: 1) automatic robustness analysis via high-performance physical simulation engines and strategies for efficient operational domain reconstruction [7], [10], 2) FoM integration for a more holistic view on operability (exemplified by critical temperature), 3) toggles for perturber placement for input signal encoding, and 4) I/O pin integrity validation. By combining these advancements, the tool empowers researchers and engineers to assess more accurate SiDB robustness efficiently and to extract critical design insights without the need for domain knowledge.

These four contributions are outlined in the following sections.

A. Automatic Robustness Analysis

The *Operational Domain Explorer* features an intuitive graphical interface modeled after *SiQAD*, ensuring a seamless transition for experienced users. It enables real-time visualization of SiDB gates, multi-dimensional parameter sweeps, and comprehensive robustness assessments for key parameters (ϵ_r, λ_{tf}, and μ_-). Fully compatible with *SiQAD*'s file format, it allows users to design logic within *SiQAD* and export it for in-depth resilience analysis.

A screenshot of the tool's interface after loading a gate designed in SiQAD is shown in Fig. 3. The left panel displays the SiDB

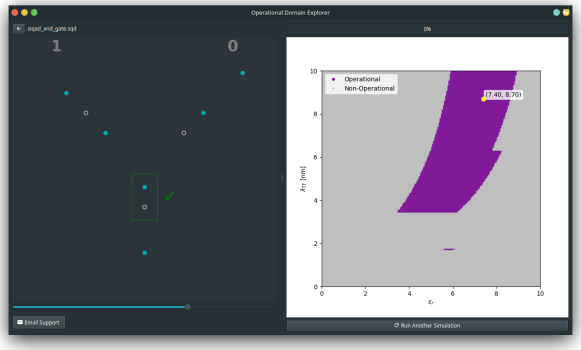


Fig. 3: GUI of the *Operational Domain Explorer*. The view shows an SiDB AND gate proposed in [6] with its charge distribution for a `10` input pattern at $\epsilon_r = 7.4$ and $\lambda_{tf} = 8.7$ on the left. Its respective operational domain in the $(\epsilon_r, \lambda_{tf})$-space is on the right, with the aforementioned sample point highlighted in yellow. Purple indicates correct logic operation.

gate layout, while the right panel visualizes the gate's operational domain across the $(\epsilon_r, \lambda_{tf})$-space, where purple and gray regions indicate *operational* and *non-operational* logic behavior, respectively. Selecting a point within this domain (e.g., the yellow marker at $\epsilon_r = 7.40$, $\lambda_{tf} = 8.70\,\text{nm}$) updates the layout view to show the corresponding charge distribution, with teal-colored dots representing negatively charged SiDBs and hollow dots denoting neutral ones. Additionally, a slider allows users to toggle through all simulated input configurations (e. g., `10`), dynamically updating the visualization. The green box around the output pair at the bottom confirms the correct logic operation for the selected sample point.

Beyond facilitating conventional robustness assessments, the tool has uncovered unexpected phenomena in SiDB operational domains. In some layouts, small, disconnected "islands" of operability appear within otherwise non-operational parameter regions. An example is evident in Fig. 3 at approximately $(\epsilon_r = 6, \lambda_{tf} = 2\,\text{nm})$, where a narrow purple region emerges from an otherwise gray expanse. Initially puzzling, these isolated operational zones suggested sporadic correct logic behavior without an immediately apparent cause. By leveraging the *Operational Domain Explorer*'s interactive capabilities, the root of this anomaly was identified: an overpopulation of charges in the input wires, which under specific parameter conditions stabilized the correct logic operation.

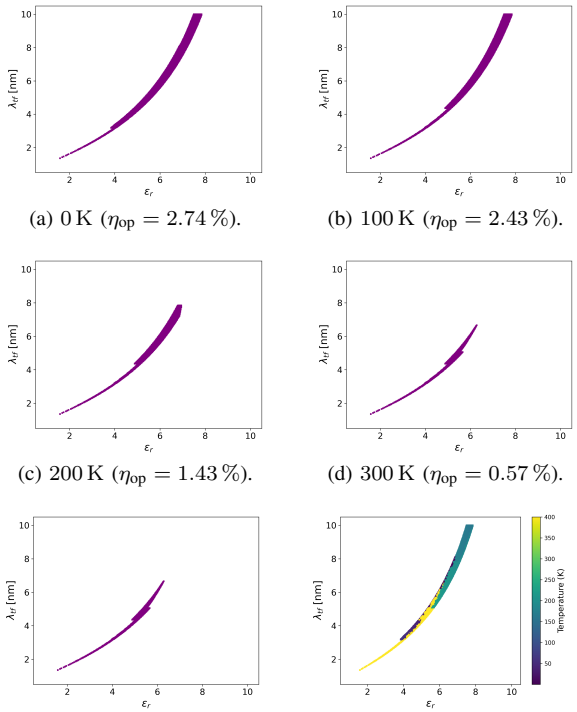
These insights demonstrate the power of automated robustness analysis in SiDB logic design, revealing subtle dependencies that would be difficult to detect through conventional methods.

B. The Critical Temperature Domain

While conventional operational domain analysis provides valuable insights into the robustness of SiDB logic gates, it typically assumes a static, low-temperature environment. In practical applications, however, thermal fluctuations significantly impact charge stability and, consequently, gate operability. To address these effects, we introduce the concept of the *Critical Temperature Domain*, which systematically evaluates the interplay between material properties and thermal robustness to ensure reliable SiDB circuit operation across a range of temperatures.

Example 4. *Fig. 4a illustrates a classical operational domain of a NAND gate with an operational ratio $\eta_{op} = 2.74\,\%$ at $0\,\text{K}$. At this temperature, the operational region remains relatively extensive. However, the underlying physical model does not account for thermal fluctuations. As temperature increases, these fluctuations introduce additional instability, impacting the charge state distributions and, consequently, the operational behavior of the gate.*

The progressive decline in operability becomes evident when examining Fig. 4b through Fig. 4d. At $100\,\text{K}$, η_{op} already drops to $2.43\,\%$, indicating a minor but noticeable reduction in stable parameter regions. As temperature further increases, this decline accelerates, with $\eta_{op} = 1.43\,\%$ at $200\,\text{K}$ and a significant drop to $0.57\,\%$ at $300\,\text{K}$. At $400\,\text{K}$, only a small fraction of the original operational domain remains viable, highlighting the severe impact of thermal perturbations on SiDB logic stability.



(a) $0\,\text{K}$ ($\eta_{\text{op}} = 2.74\,\%$). (b) $100\,\text{K}$ ($\eta_{\text{op}} = 2.43\,\%$).

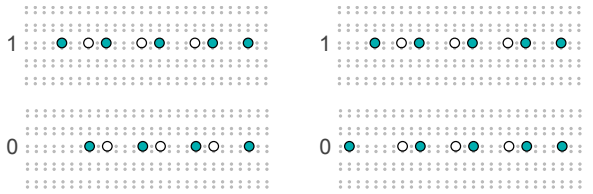
(c) $200\,\text{K}$ ($\eta_{\text{op}} = 1.43\,\%$). (d) $300\,\text{K}$ ($\eta_{\text{op}} = 0.57\,\%$).

(e) $400\,\text{K}$ ($\eta_{\text{op}} = 0.57\,\%$). (f) $0\,\text{K}$ to $400\,\text{K}$ heatmap.

Fig. 4: Operational domain plots in the $(\epsilon_r, \lambda_{tf})$-space with the corresponding operational ratio (η_{op}) of one NAND gate layout proposed in [17] at varying temperatures for $\mu_- = -0.32\,\text{eV}$. In 4a to 4e, purple indicates correct logic operation; in 4f, it is color-coded, indicating maximum stable temperature.

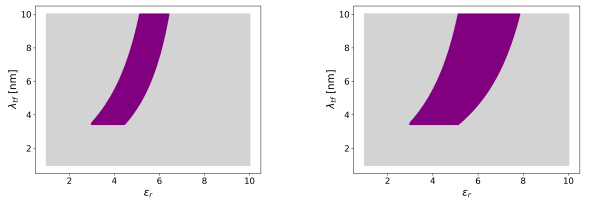
To systematically analyze and visualize these temperature-dependent effects, our tool integrates such assessments following the approach presented in [12] and renders them as intuitive heatmaps, as illustrated in Fig. 4f. It provides a comprehensive overview of the operational domain's degradation across varying temperatures. The transition from purple (indicating low temperature) to cyan and yellow (signifying increased thermal energy) illustrates the progressive reduction of the viable parameter space as thermal effects intensify. Notably, while the operational region at lower temperatures exhibits a continuous and well-defined structure, increasing thermal energy leads to fragmentation and discontinuities, revealing temperature-sensitive regions within the domain.

These findings highlight a fundamental limitation of conventional operational domain analysis: a single operational domain evaluated at $0\,\text{K}$ does not accurately capture the effects of realistic operating conditions. To address this gap, the concept of critical temperature domains offers a framework that accounts for both material properties and thermal robustness. Neglecting temperature-dependent influences risks overestimating the practical applicability of SiDB-based circuits. Consequently, future design strategies must



(a) Input encoded through the presence of a perturber. (b) Input encoded through the distance of a perturber.

Fig. 5: Alternative input signal encodings for SiDB logic.



(a) Perturber presence encoding. (b) Perturber distance encoding.

Fig. 6: The effect of both input signal encodings from Fig. 5 on the operational domain of the AND gate proposed in [6].

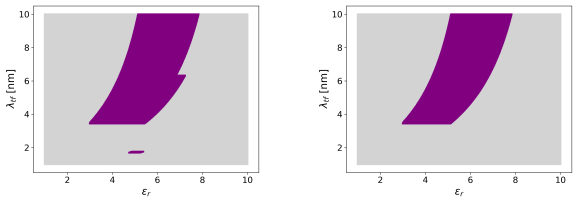
integrate thermal resilience as a key consideration to ensure the reliability of SiDB logic at operating temperatures relevant to real-world applications.

C. Input Signal Encoding

As mentioned in Section II, perturbers are individual SiDBs, which are negatively charged. This charge state can be used to exert Coulombic pressure on a wire or gate to apply an input signal. Moreover, perturbers mimic the Coulombic pressure of neighboring SiDB logic when combining several gates into larger circuitry. In the literature, two paradigms on how to use perturbers to apply input signals have emerged: 1) *Presence Encoding*: the input state is encoded through the presence or absence of a perturber. When a perturber is present, the input is set to `1`. Without a perturber, the input defaults to `0`. 2) *Distance Encoding*: the distance of the perturber dictates whether the input `0` or input `1` is applied. For input `0`, the perturber is positioned farther from the pins than for input `1`. This design choice mimics the potential effects of adjacent gates, thereby increasing the reliability of resulting robustness analyses, particularly in complex multi-gate configurations.

Example 5. *The two perturber paradigms are illustrated in Fig. 5 for an SiDB BDL wire consisting of three BDL pairs, where the perturbers can be seen on the left side. In Fig. 5a, the inputs are controlled by the presence of a perturber, i. e., its presence propagates a `1` signal along the wire, while its absence results in a `0` signal. Conversely, Fig. 5a represents the second paradigm, where the signal is controlled by the distance of the perturber from the wire. In the top wire, a close perturber encodes a `1` signal, while in the bottom wire, a more distant perturber induces a `0` signal.*

Fig. 6 displays the operational domain plots of an SiDB AND gate proposed in [6] under the different input signal encodings. Fig. 6a employs perturber presence encoding, while Fig. 6b utilized perturber distance encoding. As can be seen, the operational domain for presence encoding is significantly narrower than for distance encoding. This circumstance highlights the previously neglected importance of input signal encoding considerations when evaluating operational domains. The proposed *Operational Domain Explorer* features both methodologies to enable comprehensive analyses.



(a) Without I/O pin integrity. (b) With I/O pin integrity.

Fig. 7: The effect of I/O pin integrity on the operational domain of the AND gate proposed in [6]. Input signals are distance encoded.

D. I/O Pin Integrity

The operability of SiDB logic gates is conventionally determined by exclusively examining whether output BDL pairs correctly encode the expected result for all input patterns, as discussed in Sections II-C and III-C [6], [10]. This established approach, however, presents a significant limitation: it fails to verify the functional integrity of the I/O pins, which is essential for reliable information propagation in multi-gate circuits. However, failing I/O pins can be masked in the operational domain by otherwise correct logic behavior. In these cases, cascading these gates into larger circuits substantially diminishes the probability of successful signal transmission. Consequently, current analyses predominantly focusing on isolated gate behavior provide limited insight into the functional characteristics of larger circuits.

To address this gap, we propose to apply an I/O pin integrity verification that extends beyond the conventional assessment of output BDL pair charge states for logic correctness. It additionally validates that gate pins accurately encode the appropriate signals corresponding to the applied inputs and expected output signals. This enhanced methodology enables the delineation of operational domains based on a more stringent definition of gate operability, facilitating more accurate and representative robustness analyses of complex multi-gate configurations.

Example 6. *Fig. 7 demonstrates the impact of implementing I/O pin integrity verification on operational domain characterization. Fig. 7a depicts an operational domain without I/O pin integrity verification as conventionally done, while Fig. 7b illustrates the operational domain with verification applied. The comparison reveals that the integration of I/O pin integrity verification eliminates both the isolated domain region (island) and the right-side extension (step) from the operational domain, thereby revealing areas previously mistakenly considered operational despite I/O pin corruption.*

IV. Critical Temperature Domain Analysis

This section constitutes an evaluation of the novel methodology proposed in this work that analyzes the topology of critical temperature domains. Section IV-A goes over the experimental setup while Section IV-B presents and discusses the obtained results.

A. Experimental Setup

In this study, we investigate the topology of critical temperature domains across the $(\epsilon_r, \lambda_{tf})$-space, where $\epsilon_r \in [1, 10]$ and $\lambda_{tf} \in [1\,\text{nm}, 10\,\text{nm}]$, to assess the thermal robustness of SiDB logic gates. We selected well-established gate layouts from the literature [9] and simulated their critical temperature domains. The experiments were conducted both with and without I/O integrity checks, following the methodology outlined in Section III-D. Input signals are distance encoded. For each domain, we determined the *minimum* and *maximum* critical temperature values each gate could

TABLE I: Temperature ranges in K of the critical temperature domain in the $(\epsilon_r, \lambda_{tf})$-space, with $\epsilon_r \in [1, 10]$, $\lambda_{tf} \in [1\,\text{nm}, 10\,\text{nm}]$, and $\mu_- = -0.32\,\text{eV}$. For CT_{default}, $\epsilon_r = 5.5$, and $\lambda_{tf} = 5.0\,\text{nm}$.

Benchmark			Critical Temperature Domain Evaluation							
			without I/O pin integrity				with I/O pin integrity			
	Name	#SiDBs	CT_{min}	CT_{default}	CT_{max}	ΔCT	CT_{min}	CT_{default}	CT_{max}	ΔCT
Bestagon [9]	Str. Wire	16	0.03	4.89	> 400.00	**> 399.97**	0.03	4.89	> 400.00	**> 399.97**
	Diag. Wire	17	0.02	6.03	8.75	**8.75**	0.02	6.03	8.75	**8.73**
	Str. Inv.	19	0.01	1.03	23.01	**23.00**	0.05	1.03	23.01	**22.96**
	Diag. Inv.	19	0.01	1.59	101.63	**101.62**	0.01	1.59	88.26	**88.25**
	AND	23	0.15	59.19	256.16	**256.01**	0.06	13.36	43.69	**43.63**
	NAND	21	0.05	92.26	> 400.00	**399.95**	12.56	47.08	69.24	**56.68**
	OR	23	0.01	5.38	26.16	**26.15**	0.07	5.38	9.21	**9.14**
	NOR	21	0.02	17.82	101.17	**101.15**	0.02	17.82	21.76	**21.74**
	XOR	23	24.85	35.87	38.06	**13.21**	24.25	35.87	38.06	**13.81**
	XNOR	23	1.91	45.78	48.46	**46.55**	0.07	45.78	48.45	**48.38**
	FO2	21	< 0.01	1.46	4.65	**4.65**	< 0.01	1.46	3.37	**3.37**
	CX	29	0.01	0.85	1.00	**0.90**	0.10	0.83	1.00	**0.90**
	Double Wire	30	0.05	24.18	28.20	**28.15**	0.01	23.77	27.66	**27.65**
	HA	26	0.02	0.40	3.71	**3.69**	0.02	0.40	3.71	**3.69**

tolerate across the parameter landscape, as well as the critical temperature at default material parameters, providing a comprehensive characterization of temperature-induced stability variations.

The novel methodologies proposed in this work have been implemented in C++17 and added publicly to the *fiction* framework [18],[1] which is part of the *Munich Nanotech Toolkit* (MNT, [19]). The *Operational Domain Explorer* GUI has been implemented in PyQt6 on top of *fiction*.[2] For this experimental evaluation, all code was compiled with AppleClang 15.0.7, and run on a macOS 15.2 machine with an Apple Silicon M1 Pro SoC with 32 GB of integrated main memory.

B. Results & Discussion

Table I presents the evaluation results. The table reports the *minimum* (CT_{min}), *maximum* (CT_{max}), and *default* (CT_{default}) critical temperature values as well as the critical temperature range $\Delta CT = CT_{\text{max}} - CT_{\text{min}}$ found across the parameter landscape in K.

a) Topology of Critical Temperature Domains: An analysis of the critical temperature domains reveals that nearly all exhibit a highly uneven and rugged structure, characterized by extreme variations between CT_{min} and CT_{max}, i. e., ΔCT. This indicates that the temperature at which a gate ceases to function fluctuates significantly across the $(\epsilon_r, \lambda_{tf})$-space. Such a vast range in thermal stability was previously obscured when considering only the operational domain, which provides a binary perspective on gate functionality. The critical temperature domain, in contrast, unveils a far more intricate landscape, exposing unexpected vulnerabilities that were not apparent in traditional robustness assessments. These findings challenge previous assumptions about SiDB gate stability and highlight the necessity of incorporating thermal resilience into gate design methodologies.

b) Optimizing Material Parameters for Thermal Resilience: While most SiDB gates exhibit limited thermal stability, the analysis reveals that certain designs, such as *Str. Wire*, are capable of maintaining functionality up to room temperature. This insight was previously masked when evaluating gates solely at default material parameters, where these structures appeared far less resilient, with a CT_{default} value of only 4.89 K [12]. The critical temperature domain, however, uncovers regions in the $(\epsilon_r, \lambda_{tf})$-space where these gates exhibit significantly higher thermal stability. This suggests that instead of universally applying standard material parameters, manufacturing processes could be optimized to target regions that maximize gate resilience. Likewise, SiDB simulation and evaluation frameworks should extend beyond default parameter assumptions to capture the full spectrum of potential device performance, ensuring that designs are assessed under conditions that reflect their best possible thermal robustness.

c) Impact of I/O Integrity on Critical Temperature Domains: Beyond material optimization, another crucial factor influencing thermal robustness is the enforcement of I/O pin integrity. A significant reduction in CT_{max} is observed across most layouts when strict I/O validation is applied. For instance, *NAND*, which appears highly resilient with a CT_{max} above 400 K under relaxed conditions, drops sharply to 69.24 K when I/O pin integrity is enforced. This trend holds across various logic functions, revealing that a substantial portion of the high-temperature operational domain without integrity enforcement is an artifact of internal charge configurations rather than true functional stability. These findings underscore the necessity of rigorous validation in SiDB circuit evaluation, ensuring that robustness assessments reflect genuine operational limits rather than favorable but misleading internal states.

[1] https://github.com/cda-tum/fiction

[2] https://github.com/cda-tum/mnt-opdom-explorer

V. Conclusion

This paper extends the concept of SiDB operational domains by incorporating thermal robustness, input signal encodings, and I/O pin integrity validation into gate analysis. Implemented in the open-source *Operational Domain Explorer*, these methods enable high-resolution robustness assessments beyond default parameter assumptions. Our findings reveal that critical temperature domains are highly uneven, challenging the notion of uniform failure thresholds. Certain gates unexpectedly maintain functionality above room temperature, suggesting that fabrication could target thermally robust parameter regions. Additionally, enforcing I/O pin integrity significantly reduces temperature stability, underscoring the need for rigorous validation in SiDB evaluations. By exposing these overlooked effects, this work provides a foundation for more reliable SiDB design methodologies, emphasizing thermal-aware analysis and targeted manufacturing optimizations.

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