

Simulating Charged Defects in Silicon Dangling Bond Logic Systems to Evaluate Logic Robustness

Samuel S. H. Ng, Jeremiah Croshaw, Marcel Walter, Robert Wille, Robert Wolkow, Konrad Walus

Abstract—Recent research interest in emerging logic systems based on quantum dots has been sparked by the experimental demonstration of nanometer-scale logic devices composed of atomically sized quantum dots made of silicon dangling bonds (SiDBs), along with the availability of SiQAD, a computer-aided design tool designed for this technology. Latest design automation frameworks have enabled the synthesis of SiDB circuits that reach the size of $32 \times 10^3 \text{ nm}^2$ —orders of magnitude more complex than their hand-designed counterparts. However, current SiDB simulation engines do not take defects into account, which is important to consider for these sizable systems. This work proposes a formulation for incorporating fixed-charge simulation into established ground state models to cover an important class of defects that has a non-negligible effect on nearby SiDBs at the 10 nm scale and beyond. The formulation is validated by implementing it into SiQAD’s simulation engine and computationally reproducing experiments on multiple defect types, revealing a high level of accuracy. The new capability is applied towards studying the tolerance of several established logic gates against the introduction of a single nearby defect to establish the corresponding minimum required clearance. These findings are compared against existing metrics to form a foundation for logic robustness studies.

I. INTRODUCTION

THE pursuit of alternative logic implementations has garnered significant attention in response to the escalating challenges and rising costs associated with further miniaturization of transistors. Field-coupled nanocomputing (FCN) represents a noteworthy candidate—it defines a category of devices that operate based on field interactions, offering potential for ultra-low power consumption and high frequency operation at the atomic scale [1]–[4]. A promising implementation of FCN comes in the form of quantum dots made of silicon dangling bonds (SiDBs) on the hydrogen passivated silicon (100) 2×1 surface (H-Si(100)- 2×1), with the experimentally demonstrated capability to implement an OR gate that spans the length of less than 10 nm [5]. This groundbreaking demonstration, combined with latest developments in computer-aided design (CAD) capabilities offered by SiQAD and compatible simulators [6]–[8], has spurred wide ranging research interests

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S. S. H. Ng and K. Walus were with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada (e-mail: samueln@ece.ubc.ca; konradw@ece.ubc.ca); J. Croshaw and R. Wolkow were with the Department of Physics, University of Alberta, Edmonton, AB, Canada and Quantum Silicon Inc., Edmonton, AB, Canada (e-mail: croshaw@ualberta.ca; rwalkow@ualberta.ca); M. Walter and R. Wille were with the Chair for Design Automation, Technical University of Munich, BY, Germany (e-mail: marcel.walter@tum.de, robert.wille@tum.de). R. Wille was also with the Software Competence Center Hagenberg (SCCH) GmbH, Hagenberg, OÖ, Austria.

in the technology including the proposal of gate designs [6], [9]–[12], design automation support from the fiction framework [13], [14], an automated quantum dot gate design tool based on reinforcement learning [15], and evaluations of future applications [9], [16], [17]. However, current simulation capabilities are designed for an ideal physical environment consisting of a perfect, i.e., defect-free, silicon monocrystal substrate. While this can be justified at the individual logic gate level as gates are small enough to fit within a relatively defect-free region for experimentation purposes, the effect of defects cannot be neglected especially in light of recent design automation works that have synthesized SiDB circuits reaching the size of $32 \times 10^3 \text{ nm}^2$ [14].

Multiple types of defects may be found on the H-Si(100)- 2×1 surface, including electrically charged and neutral specimens [18]. This work proposes a formulation to capture the effects of fixed-charge defects in simulation. We implement the formulation in SimAnneal, an efficient three-state ground state charge configuration simulator offered by SiQAD, and validate the simulation results with previous experimental work [19]. We further underscore the importance of the newly introduced capability by pioneering a novel type of logic gate robustness study, where we evaluate the resilience of SiDB logic gates against the introduction of charged defects. The results are then compared with the gates’ tolerance against changes in physical parameters, a.k.a. the operational domain [6], [20].

Following this introduction, Section II provides a comprehensive overview of the physical principles and logic design endeavors related to SiDB logic. Section III describes the formulation of fixed-charge defects in the context of established ground state models. Section IV verifies the defect simulation capabilities by comparing results against physical experiments [19]. Section V then demonstrates the practical application of our methodology in assessing the resilience of logic gates against nearby charged defects. Finally, Section VI concludes our efforts and discusses future work.

II. BACKGROUND

In this section, we provide a key summary of existing literature on the fabrication of SiDBs and utilization in logic representation, the characterization of atomic defects that exert localized effects, and the evaluation of the stability of logic networks in non-ideal systems.

A. Fabrication and Logic Representation

SiDBs can be fabricated on the H-Si(100)- 2×1 surface by the removal of hydrogen atoms using a scanning probe

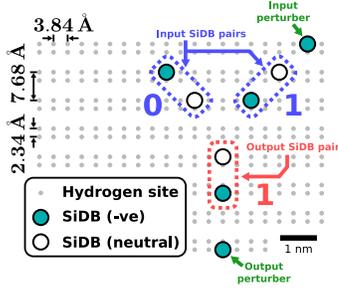


Fig. 1. Illustration of the H-Si(100)- 2×1 surface with hydrogen sites in gray, neutral SiDBs as hollow circles, and negatively charged SiDBs as teal-filled circles. The separation distances of hydrogen sites are given in the top left of the figure. The right side of the figure illustrates a reproduction of an OR gate from [6] in logic 01 configuration. The direction of logic flows from top to bottom. The input SiDB-pairs take on logic 0 by default and is set to logic 1 in the presence of input perturbers. The existence of an output perturber sets the default output SiDB-pair logic state to 0, with the logic state being pushed to 1 when one or both inputs are set to 1.

[21]; they can also be erased by re-passivating the SiDB [22]. The periodicity of the lattice structure guarantees atomically accurate hydrogen locations on the surface as illustrated in Fig. 1. SiDBs were found to exhibit quantum dot-like behavior as their energetic charge transition levels fall within the bulk band gap, allowing them to host 0, 1, or 2 electrons which correspond to positive, neutral, and negative charge states [23], [24]. In [5], Huff *et al.* experimentally demonstrated logic cells, wires, and an OR gate that represents logic states via the location of charges shared between pairs of SiDBs as shown in Fig. 1. This logic representation is later denoted binary-dot logic (BDL).

Further exploration into SiDB logic implementations came in the form of computer-aided studies with the use of SiQAD [6]. Y-shaped BDL gates implementing various common logic functions were proposed [6], [14], as were T/+ -shaped BDL gates [10]–[12] and gates that employ alternative logic representations [16], exemplifying the flexibility of the SiDB logic platform. Gate libraries and design automation frameworks have also been developed [14]. However, the effect of defects on these logic gates have yet to be extensively investigated.

B. Experimental Characterization of Defects

Material imperfections at the atomic scale have been extensively observed and characterized through advanced microscopic techniques. Scanning tunneling microscopy (STM) detects these imperfections by measuring the tunneling current, which reflects the density of states under the probe [18], [25]. Similarly, non-contact atomic force microscopy (AFM) reveals imperfections by detecting changes in the oscillation frequency of its tip in response to nearby electric charges [19]. Electrically neutral and charged defects alike can be imaged by a combination of these techniques.

Some examples of localized neutral defects are dihydride pairs and missing dimers [18]. Neutral defects may have an effect on the behavior of charges in SiDB layouts due to lattice distortion effects [26], [27], but such effects are usually pronounced only when SiDBs are adjacent to those defects. Introducing lattice effects into current SiQAD ground state

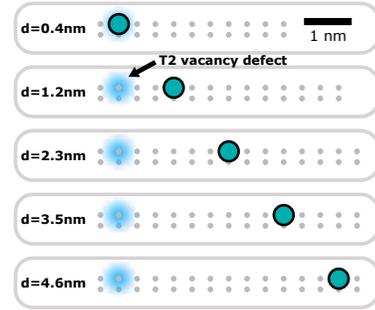


Fig. 2. Illustration of the T2 silicon vacancy defect characterization experimental setup from [19]. The defect is at a depth of 0.8 \AA below the surface and is represented by a blue halo. At each experimental step, a probe-SiDB is created at some distance from the defect, voltage sweeping experiments are performed on the SiDB, then the SiDB is removed and recreated at a different distance. The Coulombic effects exerted by the defect on the probe-SiDB weakens as distance increases, allowing parameters to be fitted.

simulators could incur a significant performance penalty. For the purpose of logic design, the undesirable effects of neutral defects may be averted by simply avoiding the placement of SiDBs adjacent to them. A special type of neutral defect is step edges, an interface between patches on the H-Si(100)- 2×1 surface where the top layer of silicon dimers is absent on one side [28]. Their main implications on logic design are: 1) the lattice dimer orientation is rotated by 90° on one side, meaning that logic circuits passing through step edges may require adaptors, and 2) changes in physical parameters between objects placed across the step edge. Step edges are challenging to capture in simulation and are currently not supported in any CAD or simulation tool that specializes in large-scale SiDB logic research. Therefore, they are also not considered in the current work.

On the other hand, charged defects like near-surface dopants and silicon vacancies can exert screened Coulombic effects on SiDB logic gates at a distance [19]. Experimental fittings for three defect types were performed in [19], including:

T1 arsenic a positively-charged arsenic dopant at 8 \AA depth;
T2 vacancy an initially unclassified negatively-charged defect at 4 \AA depth, later identified to be a silicon vacancy in [18]; and

SiDB a stray SiDB left over from incomplete passivation in the preparation of the surface.

Although surface scans via STM and AFM can reveal the locations of various types of defects, they are not capable of directly measuring the electrostatic influence that those defects would exert on SiDBs situated on the surface. To that end, Huff *et al.* employed what they denote to be a probe-SiDB as a medium to characterize the Coulombic effects from defects of interest [19]. On a patch of H-Si(100)- 2×1 surface containing a defect that is otherwise clean, the following procedure is performed:

- 1) an SiDB is created near the defect to be used as a probe medium, denoted as the probe-SiDB;
- 2) an AFM tip is positioned above the probe-SiDB;
- 3) a range of sweeping bias voltages is applied on the AFM tip and the shift in oscillating frequency is recorded, revealing a distinct charge transition of the SiDB;

4) the probe-SiDB is erased.

The process is repeated multiple times with the probe-SiDB placed at different distances, as illustrated in Fig. 2. The bias sweeps at the discrete distances reveal different offsets in the SiDB's charge transition levels, the Coulombic effects of the defect on the SiDB can be fitted via those offsets.

C. Resilience of Logic Computation Against Variations

The introduction of placement and routing methods for SiDB logic has enabled the creation of SiDB circuits at unprecedented scales for this platform technology [14]. In practice, such a sizeable circuit would likely encounter environmental variations which places a burden on the logic components to be resilient to these imperfections. Past works have studied the ability of a logic gate to abide to the intended logical behavior when subject to variations in physical parameters [6], [12], [16]. A contiguous domain of parameters within which a logic gate satisfies all truth table rows is dubbed an *operational domain*. In the screened Coulomb potential model, which is applied to experimental SiDB systems [5], [19], parameters that are relevant to the operational domain include the relative permittivity denoted ϵ_r , the Thomas-Fermi screening length denoted λ_{TF} , and the energetic difference between the neutral/negative charge transition level and the bulk Fermi level for a lone SiDB denoted μ_- . When an operational domain is plotted on the λ_{TF} vs. ϵ_r plane, changes in μ_- translate the domain along the ϵ_r axis in logarithmic scale. However, prior studies have yet to investigate the impact of charged defects on the logical stability of SiDB gates. Whereas the operational domain captures broad changes in physical parameters that can be perceived to be uniform at the spatial scale of a logic gate, a near- or on-surface charged defect can have much more localized effects that influence each SiDB with different strengths.

III. METHODOLOGY

This section constitutes the main contribution of this work. Taking the system energy formulation for classical ground state charge configurations as the starting point [5], [6], we incorporate the effects of fixed-charge defects as follows:

$$E(\vec{n}) = \sum_i V_{\text{ext}}^{(i)} n^{(i)} + \sum_i V_{\text{fc}}^{(i)} n^{(i)} + \sum_{i < j} V^{(i,j)} n^{(i)} n^{(j)} \quad (1)$$

where $V_{\text{ext}}^{(i)}$ is the sum of influences by electrostatic potential sources at the i th SiDB excepting those from defects and other SiDBs, $V_{\text{fc}}^{(i)}$ is the sum of the effects from all fixed-charge defects on each SiDB, $V^{(i,j)}$ is the screened Coulombic interaction strength between SiDBs, and $n^{(i)}$ is the charge state at each SiDB with allowed values $+1$, 0 , and -1 corresponding to the vacant, singly-charged, and doubly-charged states. This work adds the $V_{\text{fc}}^{(i)}$ term to encapsulate the Coulombic effect of defects with fixed-charges on SiDBs given by

$$V_{\text{fc}}^{(i)} = \sum_k \frac{q_0}{4\pi\epsilon_0\epsilon_r^{(k)}} \frac{m^{(k)}}{r^{(i,k)}} \exp\left(-\frac{r^{(i,k)}}{\lambda_{\text{TF}}^{(k)}}\right) \quad (2)$$

where q_0 is the elementary charge, $m^{(k)}$ is the charge state at the k th defect, ϵ_0 is the vacuum permittivity, $r^{(i,k)}$ is the

TABLE I
FITTED DEFECT PARAMETERS FROM [19]

Defect Type	Charge	Depth (Å)	ϵ_r	λ_{TF} (m)
T1 Arsenic	+1	8	9.7 ± 2.5	2.1 ± 0.7
T2 Vacancy	-1	4	10.6 ± 0.5	5.9 ± 0.6
SiDB	-1	0	4.1 ± 0.2	1.8 ± 0.1

distance between each defect and the i th SiDB, $\epsilon_r^{(k)}$ is the dielectric constant associated with each defect, and $\lambda_{\text{TF}}^{(k)}$ is the Thomas-Fermi screening length associated with each defect. To simulate these defects, the following information must be passed to a simulation engine for each defect: 1) the physical location, 2) $m^{(k)}$, 3) $\epsilon_r^{(k)}$, and 4) $\lambda_{\text{TF}}^{(k)}$. Physical parameters $\epsilon_r^{(k)}$ and $\lambda_{\text{TF}}^{(k)}$ are expected to be fitted experimentally as done in [19] or acquired from physical simulations. This formulation does not require alterations to established metastability conditions for SiDB charge states [6].

In the interest of simulation runtime, this formulation assumes that the defect being simulated maintains a fixed charge state for the physical environment in which it resides. Under extreme biases, the charged defects may take on different charge states according to the electrostatic landscape and may be subject to different metastability conditions. Capturing such effects may be of interest in future work, but is not within the scope of this formulation.

The localized band bending effects felt at the location of each SiDB can be captured by

$$V_{\text{local}}^{(i)} = -V_{\text{ext}}^{(i)} - V_{\text{fc}}^{(i)} - \sum_j V^{(i,j)} n^{(j)}. \quad (3)$$

In the presence of band bending effects, the SiDB takes a charge state that corresponds to the energetic position of its discrete charge transition levels relative to the bulk Fermi energy [23], [24]. When $V_{\text{local}}^{(i)}$ is 0, no band bending effects are present indicating an isolated SiDB devoid of external effects.

IV. MODEL VERIFICATION

To verify the correctness of the implemented formulation, we implement the model in SiQAD's SimAnneal simulator [6] and recreate Huff *et al.*'s experiments from [19] in simulation for the T1 arsenic defect, the T2 silicon vacancy defect, and an SiDB defect. Their corresponding simulation parameters are listed in Table I. We can then compare the local band bending effects (see Eq. (3)) of the probe-SiDB between simulation and experimental fittings. In simulation, the probe-SiDB is always configured as an SiDB object. In other words, in the simulator's point of view a probe-SiDB is no different from any other SiDB. The T1 arsenic and T2 vacancy defects are configured as fixed-charges with the corresponding physical parameters. Note that although the expected charge state of the SiDB defect is -1 from the experimentally tested distances, at closer distances it may be possible to observe the SiDB defect in neutral (similar to SiDB-pairs in [5]) or positive (similar to SiDB chains in [27]) states. In the simulation results presented in Fig. 3, SimAnneal returns the same results whether the SiDB defect is entered as a fixed-charge object

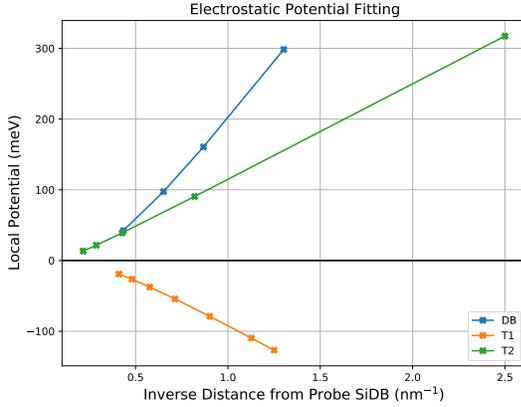


Fig. 3. Simulated local band bending effects (see Eq. (3)) of the probe-SiDB at various distances when probing the three types of defects in question. The magnitude of the electrostatic effects experienced by the probe-SiDB is expected to increase as it gets closer to the defect, which is reflected in the plot as local potentials. Defect simulation parameters $\epsilon_r^{(k)}$, $\lambda_{TF}^{(k)}$, and $m^{(k)}$ from Eq. (2) are set to those in Table I.

or an SiDB object across the tested distances. The simulation results closely align with the screened Coulomb model post-fitting as proposed by Huff *et al.* [19]. When compared to their pre-fitting data points, the simulation exhibits root mean square percentage errors of 3%, 17%, and 4%, respectively. These error values align with the variations observed in Huff *et al.*'s findings. The matching results between simulation and experimental fitting confirm the simulator's accuracy in reproducing the effects from charged defects.

V. APPLICATION IN LOGIC GATE ROBUSTNESS STUDIES

Taking advantage of the newly added defect simulation capabilities, we introduce a workflow to test a logic gate's robustness against charged defects and compare those results against their operational domains.

A. Minimum Defect Clearance for Correct Logic Computation

When we introduce a single charged defect in the vicinity of an SiDB gate, it either continues to satisfy all truth table rows or it ceases to do so. By recording the logic correctness outcome with the defect placed at various locations, we can create a map that shows where a defect can coexist with a gate and where it causes the gate to fail. We evaluate logic correctness by inspecting the logic state of the last SiDB-pair in the output wire. In Fig. 4, such a map is produced showing the locations at which a T2 vacancy defect can coexist with select components from the Bestagon gate library [14]: AND gate, dual wires, crossover, and diagonal wire. An interesting observation between the dual wires and the crossover is that the symmetrical design of the dual wires also led to a symmetrical defect tolerance map, whereas the asymmetrical crossover shows a larger clearance requirement around the left output.

For each defect location that causes a logic error, we can compute the distance between that location and its nearest SiDB to get the minimum clearance required to avoid that

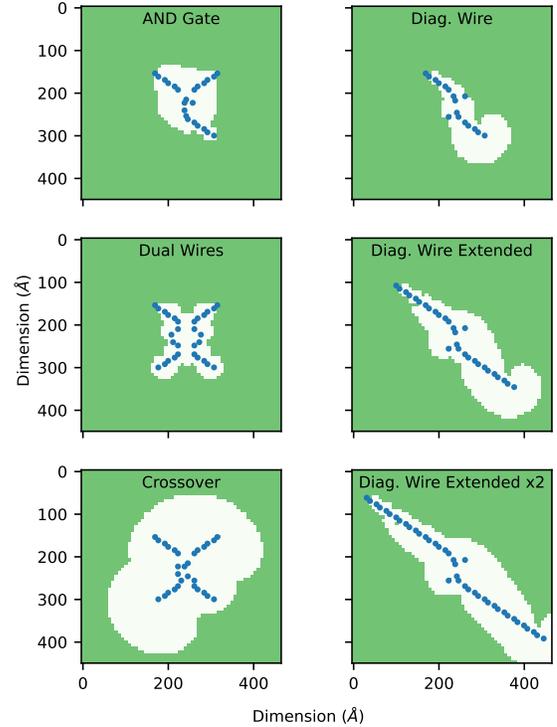


Fig. 4. Defect tolerance map for select gates from the Bestagon gate library [14] showing locations where a single T2 vacancy defect can coexist with the gates while maintaining correct logic outputs. Green filling denotes acceptable defect locations and blue dots denote SiDB locations. The top-most SiDB-pairs in all gates are input perturbers for setting the input states per [14]'s design—include just the top SiDB in the logic pair for logic 0, and just the bottom SiDB for logic 1. The panels on the right and bottom right are modified versions of the diagonal wire tile with the input and output wires extended by different lengths. The defects are simulated within a bound of $461 \times 445 \text{ nm}^2$ centered on the gate with 7.68 \AA spacing between defect placements in either direction. Inter-SiDB parameters are $\mu_- = -0.32 \text{ eV}$, $\epsilon_r = 5.6$, and $\lambda_{TF} = 5 \text{ nm}$ in SimAnneal; defect parameters are taken from Table I. Heuristic parameters in SimAnneal are: `anneal_cycles` = 10000; `num_instances` = 256 as the baseline, 1024 to verify failure thresholds, repeated as needed to reach consensus.

particular defect. Repeating this calculation for all defect locations and taking the maximum of all resulting clearance values yields the minimum defect clearance for the logic gate to remain operational for that defect type. In Table II, we report the minimum defect clearance for logic gates from the Bestagon gate library [14] in the presence of T1 arsenic at a depth of 8 \AA and T2 vacancy at a depth of 4 \AA . All Bestagon components are included excepting the half adder as it fails to function throughout the entire simulation grid. Across all combinations of gates and defects, the defect placement bounds and intervals as well as heuristic SimAnneal settings are consistent with those reported in the caption of Fig. 4. For inter-SiDB parameters, physical parameters are set to those specified by the Bestagon library [14]: $\mu_- = -0.32 \text{ eV}$, $\epsilon_r = 5.6$, and $\lambda_{TF} = 5 \text{ nm}$; the fixed-charge defects take the parameters from Table I. The planar distance is reported, meaning the distance between an SiDB and the defect's location projected onto the same plane as the SiDB. The true distance is the hypotenuse computed from the reported planar distance and defect depth. The Bestagon gate library

is chosen for this study because all gates in the library share standard locations for input and output wires, which provides a fair platform for robustness comparison. We observe that the required defect clearances are generally < 10 nm for the Bestagon gates with a few outliers.

We further investigated the defect tolerance maps for modified versions of the diagonal wire with the input and output wires extended by 3 and 6 SiDB-pairs as shown in the right and bottom right panes of Fig. 4, respectively. The exclusion region tracks closely to the input wire in all variants of the diagonal wire, but a larger exclusion zone exists near the output wire. We suspect the cause to be the statically placed output perturber as opposed to the input perturbers which shift locations based on input state [14]. In the presence of the output perturber, a nearby negatively charged defect may only require a small bias to make logic 0 a more likely outcome in the design of this component. Starting from a clearance requirement of 7.2 nm for the original diagonal wire, at 3 and 6 SiDB-pair extensions the defect clearance increases to 7.7 nm and 7.9 nm, respectively. Note that although the exclusion region clips the border of the simulated grid in the latter case in Fig. 4, the same clearance value was achieved after expanding the simulation grid. We attribute the low degradation in clearance requirements to the effects of screening which exponentially attenuates Coulomb interactions. This bodes well for future investigations into multi-gate logic stability as the Coulombic effects between gates can be attenuated by placing sufficiently long wires between components.

Another interesting observation is the existence of a “dimple” in the white region above the bottommost SiDB-pair across all three variants of the diagonal wire, meaning that the wire is more robust against the defect in that region. We believe that the statically placed output perturber to also be the cause here, creating a sweet spot in the defect tolerance map where the negatively charged defect can exist closer to the wire than usual and still maintain correct logic outputs. If the output perturber was replaced by a longer wire or a different logic component, we expect the dimple to disappear. This result may serve as motivation for future work to consider alternative output perturber designs to more accurately capture the Coulombic effects that an output wire would exert on the logic component.

B. Comparison Against Other Robustness Metrics

As discussed in Section II, existing studies on SiDB logic have not put a major emphasis on logic stability in the presence of environmental variations, with relevant efforts mainly focused on operational domains which captures variations that affect an entire logic gate uniformly [6], [12]. Since the effects of near-surface charged defects are much more localized, it is important to evaluate the newly proposed defect clearance against existing robustness metrics. Past works that have studied operational domains have presented the results graphically [6], [12], [16] without offering a numeric figure of merit, necessitating an original quantification scheme for this comparison. In SiDB logic gate literature, each logic gate targets a specific set of physical parameters including

TABLE II
DEFECT CLEARANCE AND OPERATIONAL DOMAIN OF BESTAGON GATES

Bestagon Gates [14]	Defect Clearance (nm)		Operational Domain	
	T1 Arsenic	T2 Vacancy	μ_- const.	$\mu_- \pm 10\%$
Wire Diag	4.1	7.2	67.0%	36.3%
Wire	4.5	7.9	64.5%	36.3%
INV	6.9	12.0	33.8%	11.5%
OR	3.3	7.2	34.0%	9.8%
AND	1.7	6.2	16.5%	0.0%
Dual Wires	3.4	3.2	14.5%	0.0%
INV Diag	5.8	8.3	13.5%	8.8%
NOR	4.9	7.1	11.5%	0.0%
Fanout-2	6.2	13.7	8.5%	0.0%
NAND	5.0	6.1	6.0%	0.0%
XNOR	5.0	5.8	6.0%	0.0%
XOR	5.4	9.6	4.0%	0.0%
Crossover	9.0	12.9	0.5%	0.0%

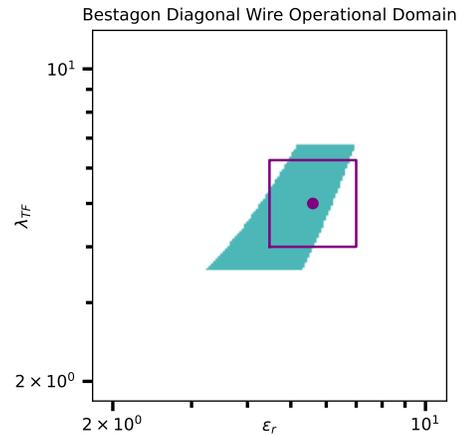


Fig. 5. Operational domain of the diagonal wire tile from the Bestagon gate library [14] with $\mu_- = -0.32$ eV simulated with 150 points in each dimension in logarithmic spacing. The teal-filled domain represents parameters that yield successful logic outputs for the wire; the purple point represents the ϵ_r and λ_{TF} parameters that the wire was designed for; the square centered on that point represents the parameter neighborhood considered by this work which is ± 0.25 of the target parameters in log space. The SimAnneal heuristic parameters are set to `anneal_cycle = 10000` and `num_instances = 512`.

μ_- , ϵ_r , and λ_{TF} . A physical H-Si(100)- 2×1 specimen that is tuned to the same set of physical parameters would ideally only exhibit minor deviation across the surface. Therefore, we posit that the most relevant section of the operational domain is the nearest neighborhood around the gate’s targeted parameters. For this study, we have opted to focus on the parameter neighborhood of ϵ_r , λ_{TF} , and μ_- that the Bestagon components are designed for. The bounds are set to ± 0.25 for ϵ_r and λ_{TF} in log space with a discrete parameter grid of 20 by 20 in log-log scale. Fig. 5 illustrates the operational domain of the Bestagon diagonal wire [14] at $\mu_- = -0.32$ eV, the considered parameter neighborhood is also highlighted. The bounds for μ_- are set to ± 0.1 in log space as we found ± 0.25 to yield no working results. We believe that the chosen μ_- bounds remain to be physically relevant as the bulk dopant concentration across the sample can be prepared to be relatively stable [25]. As previously mentioned, broad variations in μ_- shifts the operational domain in the ϵ_r

direction in log scale. Therefore, the operational domain with μ_- consideration can be constructed by taking the intersection of the λ_{TF} vs. ϵ_r domain at the μ_- bounds.

We quantify the robustness of each gate by taking the logical success rate within the inspected parameter neighborhood. The results are included in Table II with the “ μ_- const.” and “ $\mu_- \pm 10\%$ ” columns showing success rates without and with μ_- variation, respectively. We observe that many gates from the Bestagon library are highly sensitive to μ_- variations, with more than half of them achieving 0% success rate in the chosen μ_- bounds. This is a result of the operational domains having insufficient width in the ϵ_r axis to withstand domain translations caused by μ_- variations. This may be indicative that future logic design works should prioritize ϵ_r robustness as having higher ϵ_r tolerance also benefits μ_- tolerance.

We do not find a clear correlation between the overall trends for defect clearance and operational domain. As previously mentioned, operational domain studies apply deviations from the targeted parameters uniformly on the entire logic gate, whereas the introduction of defects exert highly localized effects thanks to the exponential effects of screening (see Eq. (2)). If we inspect the local potential influences of the T2 vacancy defect plotted in Fig. 3, as the probe-SiDB moves from 0.4 nm to 4.6 nm, the Coulombic repulsion experienced by the probe-SiDB is also reduced by a factor of > 20 , showing how rapidly the defect’s influence falls off.

VI. CONCLUSION

This work has proposed a formulation to simulate fixed-charge defects in SiDB systems, and demonstrated its accuracy by implementing it in SiQAD’s ground state simulator and comparing the results with past experimental findings. The ability to simulate defects in line with experimental findings for the first time bring a valuable tool for experimentalists and logic designers alike. Experimentalists have gained the ability to more accurately predict the behavior of SiDB layouts in the presence of charged defects and adjust the layouts accordingly before carrying out experiments. Designers may now explore the sensitivity of their circuit designs in the presence of nearby defects. Automated circuit designers [15] may also make use of defect simulation capabilities to optimize gates with nearby defects in mind. Future works have the opportunity to further add to the simulation capabilities by considering the incorporation of a dynamic charge state model that is aware of the defects’ energetic charge transition levels. Metastability conditions of these dynamic defect charge states may take inspiration from the equivalent conditions proposed for SiDBs in [6]. The simulation of neutral defects may also be of interest, but they may involve more drastic changes to simulator implementation since the energetic effects from lattice distortions may have a dependence on the charge configuration [26], which might necessitate a re-computation for every charge reconfiguration.

In assessing the robustness of logic gate designs, this study promptly illustrates the application of the methodology in evaluating the resilience of logic gates from the Bestagon gate library [14] against the introduction of a single charged defect in its vicinity, leading to a defect clearance value that can

be assigned to each logic gate. We have also investigated the defect clearances of a diagonal wire component with extended input and output wires, observing that the defect clearance requirement did not increase significantly. Gate library designers can use the presented methodologies to identify opportunities for further improvements. This also creates research opportunities for the design automation community at multiple steps of the design flow. At the logic synthesis step, gates with high clearance requirements can be associated with high costs in order to reduce the use of those gates. In the placement and routing step, awareness of defect clearance requirements can ensure that the resulting circuits are compatible with the defect landscape.

We have also examined the operational domain of the Bestagon gates by varying the physical parameters λ_{TF} , ϵ_r , and μ_- [6]. We quantify the operational domains by introducing an original figure of merit which evaluates the proportion of operational parameter sets that fall within a parameter neighborhood for the physical parameters that the gates were designed for. Simulation results show that Bestagon gates are very sensitive to variations in μ_- , underscoring an important consideration for gate designers in guiding future design strategies. Interestingly, our analysis reveals a lack of correlation between operational domains and minimum defect clearance values, highlighting a complex interplay between the broad physical effects encapsulated by operational domains and the localized influences exerted by charged defects. This discovery paves the way for future research, emphasizing the need for comprehensive models that evaluate multiple robustness metrics in tandem. Such an approach is crucial for advancing our understanding and development of more resilient SiDB logic systems.

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