Three-Input NPN Class Gate Library for Atomic Silicon Quantum Dots

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***Abstract*—This article proposes a complete 3-input gate library using atomic silicon quantum-dots made of silicon dangling bonds (SiDBs). This emerging technology aims to achieve ultra-low energy dissipation and high-density integration using field interactions rather than the flow of electric current. Our main contribution is a SiDB gate library of ten logic gates to cover all 256 3-input Boolean functions by utilizing NPN equivalence classes. Finally, the results present detailed properties of our designs and discuss their robustness against environmental variations. We use SiQAD, a state-of-art CAD tool specialized for SiDB technologies, for simulation and verification.**

***Index Terms*—Atomic Silicon Quantum-dot, Gate Library, Three-input Gates, Silicon Dangling Bonds, and SiQAD**

I. Introduction

Modern complementary metal-oxide-semiconductor (CMOS) technologies are reaching physical scaling limitations, sparking the emergence of novel computational technologies such as *Field-coupled Nanocomputing* (FCN) [1]. FCN promises ultra-low energy dissipation and high-density integration by the use of field interactions in the system rather than the flow of electric current. Multiple physical FCN implementations have been proposed. Among the most well-known are nanomagnetic logic (NML) and quantum-dot cellular automata (QCA) [1]. The former relies on magnetic field interaction between regular arrays of nanomagnets and the latter on electric field interaction in cells made of quantum dots. One promising novel approach to perform FCN logic that has gained momentum in recent years due to breakthroughs in fabrication capabilities is the use of *Silicon Dangling Bonds* (SiDBs) acting as quantum dots at the limit of scaling [2]–[4]. This application of SiDBs is also dubbed *Atomic Silicon Quantum Dots*.

FCN opens new opportunities for logic gate design. While CMOS gate design uses series-parallel association of transistors to build primitive logic operations such as AND, OR, and Inverter, QCA and NML use Majority and Inverter gates as logic primitives. It is straightforward to implement AND and OR gates using a Majority gate. Nevertheless, it is costly to implement XOR or multiplexers. SiDBs introduce more freedom to design logic gate primitives by controlling the position, distribution, and orientation of individual SiDBs. Evidence of the advantages of SiDB logic implementation comes in the form of a recent physical demonstration of a sub-$30\,\mathrm{nm}^2$ charge-based logic OR gate and nanoscale wire components [4]. The demonstrated layouts encode logic states by the location of a charge in a pair of SiDBs, dubbed *Binary-Dot Logic* (BDL).

The flexibility offered by the new platform also bears unique new challenges, warranting further exploration, which was made possible by *SiQAD* [5], a CAD tool for the design and simulation of SiDB logic layouts calibrated to experimental results. The tool has fueled multiple recent works to introduce BDL logic gates with a variety of layout topologies and implemented components: wire crossings [5], [6], Y-shaped [5] and T-shaped [6] 2-input gates, as well as some 3-input gates (Xor3 [6], Majority [6], AndOr [7], OrAnd [7]). Although SiDB logic development is still in early stages, opportunities to offer forward-looking design methodologies that optimize the area footprint of future SiDB circuit implementations have already been identified. For example, even though 3-input gates have a tendency to occupy more space than 2-input gates [6], [7], the logic expressiveness of some 3-input gate classes promises representations that require fewer logic elements and, thus, might reduce the overall layout size. To this end, the creation of novel gates can be achieved by careful tuning of the angles and placements of input and output BDL wires as well as additional logic structures at the center of the gates, as detailed in later sections. This freedom in SiDB placement and the ability to create a large number of primitive logic gates pose a major advantage for the SiDB platform in comparison with other FCN technologies that rely on patterned arrays for the placement of their elementary devices.

This work proposes a SiDB gate library of ten logic gates to cover all 3-input Boolean functions by utilizing NPN equivalence classes. Intuitively speaking, two Boolean functions are said to be NPN-equivalent if there exists an optional negation of the primary inputs, a permutation of the primary inputs as well as an optional negation of the primary output such that the functions are equivalent. NPN equivalence is discussed in more detail in Section III. In this paper, we introduce seven novel highly expressive gates (in addition to three previously

presented) that correspond to one NPN equivalence class each. The potential benefits of the respective Boolean functions have been demonstrated in recent logic synthesis applications [8].

Moreover, our library of compact 3-input cells uses fewer than 20 SiDBs per gate. The SiDB implementations were designed using SiQAD and carefully simulated with its state-of-the-art physical simulator to ensure their intended behavior. Design and simulation files for all gates are available in a public repository.[1]

We organize this paper as follows. In Section II, we review the physical background on SiDBs, logic demonstrations on this platform, and computational works which enable the design and simulation of SiDB logic gates. In Section III, we explain the significance of expressive 3-input gate classes and present our full 3-input NPN gate library for atomic silicon quantum dots. In Section IV, we present detailed properties of our designs and discuss their robustness against environmental variations. Finally, in Section V, we conclude our work and discuss future opportunities in large-scale SiDB logic designs that make use of our proposed gates.

II. SiDB Logic Background and Design Methods

SiDB logic design is an emerging field in which physical design rules, design flows, and testing procedures are all undergoing rapid development. Despite its hurdles, the implementation of the FCN concept via SiDBs promises an unrivaled level of flexibility and versatility. In this section, we review existing experimental and computational studies on the atomic silicon quantum dot platform, the state-of-the-art CAD tool SiQAD developed for this technology, and SiDB logic gates proposed in recent literature.

A. The Elementary Device

Experimental demonstration of FCN logic gates fabricated with SiDBs sparked interests in this revolutionary logic platform at the atomic scale [4]. To fully appreciate the novelty of this platform and the platform-specific constraints, it is important to review its key physical properties as well as its logic implementation capabilities.

The SiDBs in question exist on the surface of hydrogen-passivated silicon (100) 2×1 (H-Si(100)-2×1) and are created by the application of a localized current at a hydrogen site to break the H-Si bond, leaving behind a SiDB [2], [3]. Each SiDB may hold 0 to 2 electrons, corresponding to positive, neutral, and negative charge states. The charge state taken on by a SiDB is dependent on the bulk doping concentration and local electric potentials that it is exposed to. Experimental implementations of SiDB FCN logic were exclusively carried out with n-doped silicon bulk, causing a tendency for the SiDBs to take on negative or neutral charge states depending on placement and environmental biases. SiDBs can be fabricated at atomically precise locations on the H-Si(100)-2×1 surface, as illustrated in Fig. 1(a).

Taking advantage of these physical properties, Huff *et al.* experimentally demonstrated the implementation of SiDB FCN logic [4]. It was shown that a carefully positioned SiDB pair would share a single negative charge and that logic states can be represented by the position of this charge. Placing multiple SiDB pairs in series allows the construction of logic wires, as illustrated in Fig. 1(a–b) where a SiDB pair is indicated in green. The existence of *perturbers* on either side of the BDL wires, shaded in orange, is to be noted. These are SiDBs that act to exert Coulombic repulsion on the logic structure in order to set the logic state in these experimental setups. In the future, logic states in SiDB structures are expected to be set by interfacing electronic components at the periphery of the circuits [4], [5].

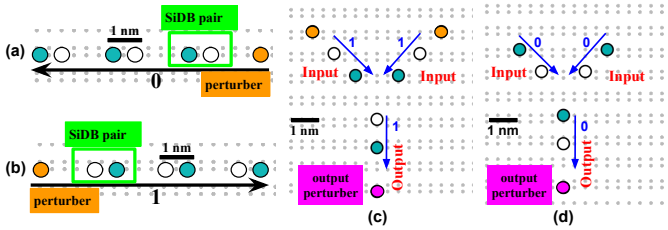

Fig. 1. Fundamental building blocks: (a) wire propagating signal 0, (b) wire propagating signal 1, (c) Y-shape 2-input OR gate, input = 11, and (d) Y-shape 2-input OR gate, input = 00.

Also demonstrated by Huff *et al.* was a BDL 2-input OR gate with sub-30 nm^2 area usage. Reproduction of the OR gate in 11 and 00 input configurations are shown in Fig. 1(c–d). Similar to BDL wires, the input states are set by the existence of perturbers. In addition, a perturber at the output acts to emulate the existence of a prolonged output BDL wire and, thus, ensures the output SiDB pair logic state to be 0 at the 00 input state. These experimental demonstrations inspire further research into this space, which requires physical models and CAD tools as reviewed in the next section.

B. CAD and Physical Models

Exploration of this novel logic platform extends beyond purely experimental work. *SiQAD* is a CAD tool specialized in the design and simulation of SiDB systems [5]. Its design tools allow users to create SiDB and electrode layouts and to perform physical simulations of the designs. The simulation engines are physically-informed and calibrated to experimental results, allowing us to explore the novel design space and to offer foundational findings for this emerging research field.

Among the available simulation tools, of most interest to SiDB FCN design is SiQAD's ground state charge configuration simulation models as SiDB's logic representation generally relies on ground state operation. SiQAD's model defines the ground state as the lowest energy metastable charge configuration [5]. The configuration energy model takes the screened Coulombic potentials, in line with experimental findings [4]. There are three physical parameters in the model of particular interest: the relative permittivity (ϵ_r), the Thomas-Fermi screening length (λ_{TF}), and the chemical potential which roughly models influences from bulk doping levels (μ_-). The actual values of these parameters are dependent on the exact

[1] https://github.com/lesc-ufv/Three-Input_Gates_for_SiDB

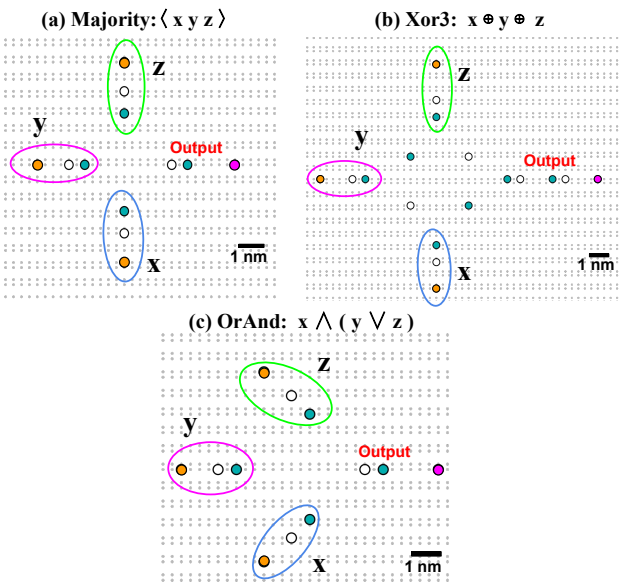

Fig. 2. Prior novel 3-input designs with the inputs circled and the outputs labeled. (a) Majority [6]. (b) Xor3 [6]. (c) OrAnd [7].

physical surface preparation procedures. In this work, we assume $\epsilon_r = 5.6$ and $\lambda_{\text{TF}} = 5\,\text{nm}$ unless otherwise specified, in line with experimentally fitted parameters [4]; μ_- is subject to more freedom, where the exact value is specified for each simulation presented [5].

SiQAD offers two simulators that implement the ground state model: *ExhaustiveGS*, which exhaustively computes every possible charge configuration available in a given SiDB layout to find the ground state configuration; and *SimAnenal*, which is a heuristic implementation of the model with a much lower runtime that enables the exploration of larger SiDB layouts. This work uses SimAnneal for the simulation results presented unless otherwise specified.

C. SiDB Logic Gate Designs

SiQAD enables rapid prototyping of logic gate designs before physical production. Multiple works have used SiQAD to propose novel logic gate designs covering 2- and 3-input gate designs. For 2-input gates, the literature has proposed both Y-shaped layouts [5] abiding to Huff *et al.*'s demonstrated work and innovative T-shaped layouts [6]. Similar area costs are achieved with either construction. 3-input designs have also been proposed without a significant increase in area usage, opening the door to more compact circuit designs. Fig. 2 depicts multiple existing 3-input gate designs from the literature and their respective Boolean expressions, including Majority [6], Xor3 [6], and OrAnd [7] gate implementations.

A number of SiDB circuits composed of more than one gate can also be found in literature, e.g., a half-adder [5], a 2-input multiplexer [5], a full-adder [6], as well as our previous AndOr and OrAnd designs [7]. Multi-gate circuits are difficult to design using existing tooling and design rules. Current gate designs are created and examined in isolation; when used in composed circuit layouts, Coulombic influence from wires and nearby gates may cause individual gates to malfunction, requiring further tweaks to adapt to their operating environment. Modes of malfunctioning may include: (1) inputs and outputs of connected gates interfering with each other; (2) Coulombic pressure from nearby components causing an insufficient charge count in a logic component; and (3) Coulombic repulsion biasing the gate into unintended charge configurations.

These difficulties motivate further development of 3-input gates as their employment can lead to reduced overall gate counts in circuits, hence reducing the amount of fine-tuning needed to bring a circuit to operational state.

III. Complete 3-Input NPN SiDB Gate Library

In this section, we present and discuss a complete 3-input NPN gate library for atomic silicon quantum dots that extends our prior work to a total of 10 novel highly expressive logic gate implementations.

A. Motivation for NPN Classes

Conventional standard gate libraries provide gate implementations of simple logic functions like AND, OR, NAND, NOR, XOR, XNOR, etc. However, even though these gates are the most common, they might not be the most *expressive*. The term expressiveness in this regard defines a relation between the number of gates of a certain type (plus inverters, which are not counted) that are needed to implement a given set of complex combinational circuits. The lower the number of gates that are needed of a particular type, the higher is said gate type's expressiveness.

Intuitively speaking, having only AND gates (and inverters) available, implementing any set of complex circuits, takes more gates than implementing the same circuits with only Majority gates (and inverters). This conjecture is easily justified due to the fact that Majority is able to implement both AND and OR by setting one of its inputs constant 0 or 1, respectively. Consequently, Majority covers a super-set of AND's domain and is, thus, more expressive.

Marakkalage *et al.* experimentally evaluated the expressiveness of all 3-input Boolean functions by means of their canonical *NPN class* representatives [8]. Two Boolean functions $f(x_1, \ldots, x_n)$ and $g(x_1, \ldots, x_n)$ are NPN-equivalent if $f(x_1, \ldots, x_n) \equiv \dot{g}(\pi(\dot{x}_1, \ldots, \dot{x}_n))$, where π represents an arbitrary permutation and $\dot{x}$ denotes an optional inversion of x. That is, if one function can be transformed to be equivalent to the other by optionally inverting inputs and the output as well as permuting the inputs. This is a powerful concept as it tremendously reduces the number of, e.g., all 3-input Boolean functions from 256 to only 14 NPN classes, 4 of which can be ignored as they do not utilize all three input variables; resulting in 10 true 3-input NPN classes.

In many nanotechnologies such as NML, input permutation, as well as signal inversion, are trivial, which motivated the notion of NPN equivalence in the first place. The same conjecture holds for SiDBs: signal permutation can be handled

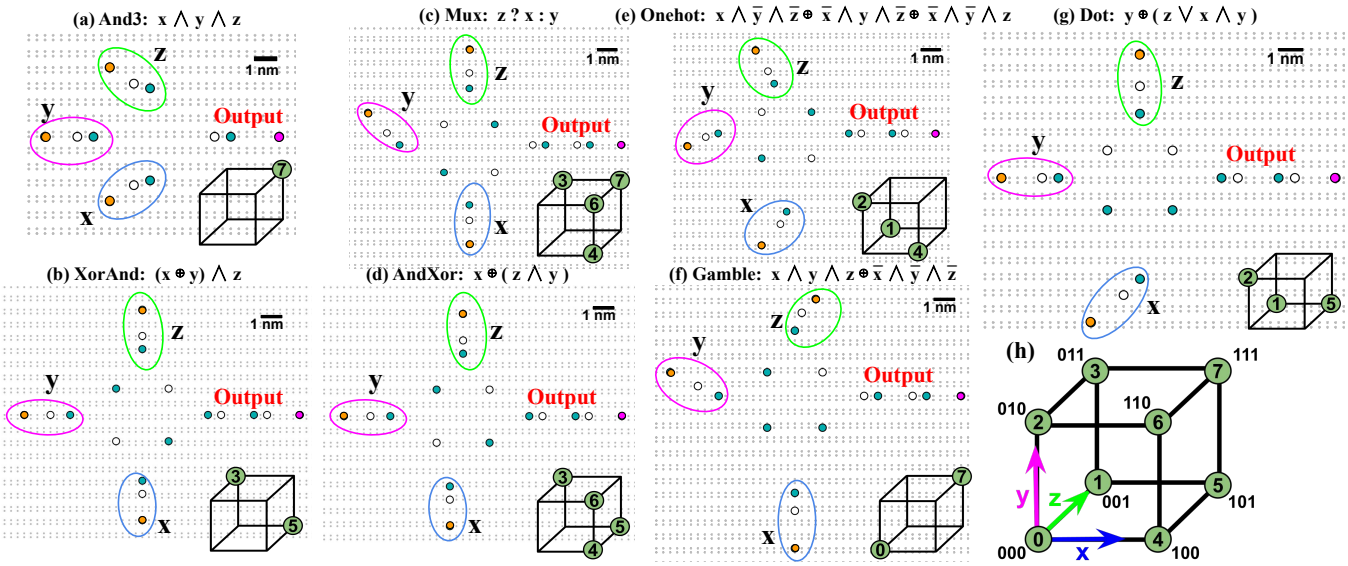

Fig. 3. Our novel 3-input designs. (a) And3, (b) XorAnd, (c) Mux, (d) AndXor, (e) Onehot, (f) Gamble, (g) Dot, and (h) 3-input Cube $f(x, y, z)$.

by routing algorithms while it has been shown that signal inversion is realizable within wire segments by adjusting the number of utilized DB pairs pairs [5].

The choice between simple and complex gates is strongly dependent on the target technology. For instance, simple 2-input AND/XOR gates perform better than complex gates in CMOS technology [9]. Nevertheless, Majority-based gate libraries are more suitable for NML and QCA technologies [1]. In the SiDB scenario, several fundamental issues such as gate design, interconnection, and mapping are still open problems. While CMOS complex cell design is based on series-parallel or pass-transistor logic topologies, SiDB gate design explores geometric properties such as angles and distances between SiDB dots. In this sense, more complex gates such as 3-input ones reduce reconvergences and internalize some fanout and fanin issues.

Marakkalage *et al.* took one (canonical) representative from each class and used it in combination with inverters to implement the EPFL benchmark suite [10], which yielded surprising results. Even though Majority is used as an elementary building block in various emerging computation technologies like QCA, NML, AQFP, etc., other 3-input functions, e.g., Dot which was found to require $14\,\%$ fewer gates, exceed its expressiveness (cf. [8] for the full discussion).

B. NPN Gate Implementations

Despite their expressive power, to the best of the authors' knowledge, there is currently no computational technology that applies 3-input NPN class representatives as elementary building blocks. This section addresses this shortcoming by providing implementations in the form of SiDB gates. Since SiDB technology is in its infancy, the design of gates is still largely a simulator-based empirical process that requires experience and systematic exploration. As mentioned in Section II-A, designers face various challenges in the process of creating SiDB logic gate designs due to the potential sensitivity of gates to external biases. The use of perturbers serve to simulate the influence of input and output wires exerted on the gate.

The angles and distances between SiDB-based building blocks are fundamental for the design. We established a guideline to design novel gates based on two 3-input gates, Majority and Xor3 [6]. We have explored the solution space by varying three parameters: (1) the distance between the DB pairs (intra-DB); (2) the distance between two DBs that compose a pair (inter-DB); and (3) the angles of the DB pairs from the inputs. And3 is based on Majority. The remaining gates are based on Xor3, varying the three parameters, as shown in Fig. 3. More details about this process can be found in our previous work [7].

SiDB structures could be found which implement all 3-input NPN class representatives. These are shown in Fig. 3. The subfigures (a–g) represent our novel designs, where the computed functions of these gates are given as Boolean expressions in the figure captions and in cube notation in the bottom-right corner of each design. This cube follows the configuration and orientation guidelines given by the bigger cube shown in Fig. 3(h). The Boolean functions And3 (Fig. 3(a)), Onehot (Fig. 3(e)), and Gamble (Fig. 3(f)) are symmetrical such that their input permutations are irrelevant. Similarly, XorAnd (Fig. 3(b)) and AndXor (Fig. 3(d)) are partially symmetrical in their x and y inputs. These properties should facilitate their designs' incorporation with placement and routing algorithms.

IV. Experimental Evaluation

We used SiQAD to design and verify all of our 3-input NPN gate designs. We took an empirical approach that consists of modifying angles and distances from prior designs to achieve working novel logic gates. We evaluated the SiDB count and

TABLE I
INVESTIGATING THE DB-BASED CELLS

Gate	Function	Area (nm^2)	SiDB Count
Y-shape Or2 [6]	$x \vee y$	29	6
T-shape Or2 [5]	$x \vee y$	68	8
And3	$x \wedge y \wedge z$	75	8
Majority [6]	$\langle xyz \rangle$	90	8
OrAnd [7]	$x \wedge (y \vee z)$	91	8
Onehot	$x \wedge \bar{y} \wedge \bar{z} \oplus \bar{x} \wedge y \wedge \bar{z} \oplus \bar{x} \wedge \bar{y} \wedge z$	191	14
Xor3 [6]	$x \oplus y \oplus z$	196	14
Mux	$x \ ? \ y : z$	198	14
AndXor	$x \oplus y \wedge z$	204	14
XorAnd	$x \wedge (y \oplus z)$	204	14
Dot	$x \oplus (z \vee x \wedge y)$	208	14
Gamble	$x \wedge y \wedge z \oplus \bar{x} \wedge \bar{y} \wedge \bar{z}$	230	14

area costs of the proposed layouts which are listed in Table I. Gates that are taken from literature have the corresponding citations included in the table. It is to be noted that we did not include the input and output perturbers in the SiDB count because in actual integrated circuit designs, the input and output logic will be carried by wires rather than being set by perturbers.

A. Properties of Implemented Gates

All proposed 3-input NPN gates require between 8 and 14 SiDBs, while the Y-shape and T-shape 2-input gates have 8 SiDBs on average. Although our 3-input NPN gates occupy a slightly larger area to ensure correct functionality, the smallest of them still use the same number of SiDBs as the T-shaped 2-input OR gate from the literature [6]. It is to be noted that the number and positioning of the inputs certainly influence the gates' size. The average area for our 3-input NPN gates ($148\,\mathrm{nm}^2$) is 3 times higher than the average area for the 2-input gates ($48\,\mathrm{nm}^2$), without considering the area costs for wire connections that would be needed to connect gates within a circuit layout. We assume this trade-off to be acceptable since it is expected that highly expressive 3-input gates can ultimately reduce the number of gates required in synthesized circuits at a large scale as, e.g., shown by Marakkalage *et al.* on the logic level [8].

B. Operational Domain

Another important aspect in the design of SiDB logic gates is their operational domain—a set of physical parameters within which the ground state charge configuration represents the desired correct gate output. In the fabrication process, there may appear adverse effects [11] such as variations in bulk dopant concentration, near-surface or surface defects, and stray dopants. They cause variations in local physical parameters which may lead to logic gate malfunction. Gates that can operate over a larger set of physical parameters entail improved robustness against such environmental imperfections. Fig. 4 shows the operational domain of the proposed And3 gate, depicted in Fig. 3(a), acquired by sweeping through ϵ_r and λ_{TF} parameters in SiQAD's ExhaustiveGS simulation for all input combinations and comparing the results against desired charge configurations for correct logical operation. Each input combination may operate over a different domain; the actual

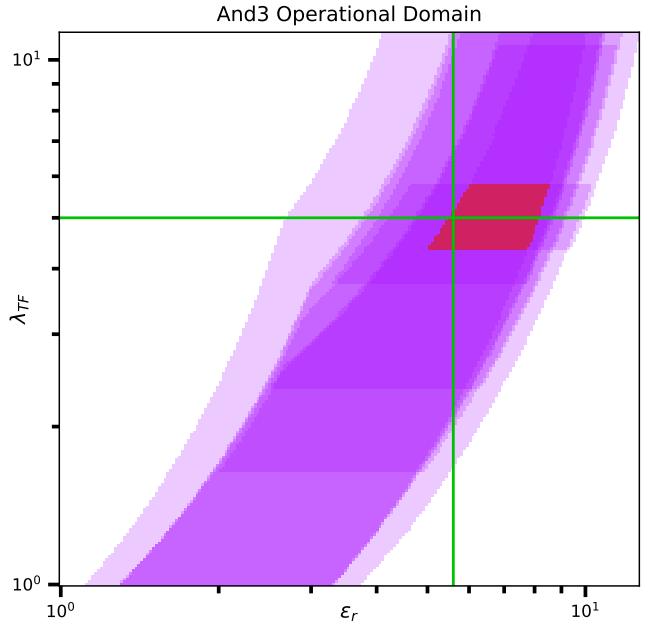

Fig. 4. Operational domain of our proposed And3 gate (ref. Fig. 3(a)) acquired from SiQAD ground state simulations by sweeping ϵ_r and λ_{TF} values at $\mu_- = -0.25\,\mathrm{eV}$. All input combinations are superimposed and depicted in purple. The intersection of the domains of all input combinations, highlighted in red, is the actual operational domain. Green lines are drawn at $\epsilon_r = 5.6$ and $\lambda_{\mathrm{TF}} = 5\,\mathrm{nm}$ to indicate the parameters that the gate was designed for.

operational domain of the entire gate is the intersection of all input combinations shown in red. It can be seen that the target physical parameters that the gate was designed for, $\epsilon_r = 5.6$ and $\lambda_{\mathrm{TF}} = 5\,\mathrm{nm}$, lie within the operational domain. However, a lower ϵ_r could cause the gate to malfunction. A worthwhile future investigation will be to develop design rules to methodically design gates with larger operational domains. Note that it is also possible to perform this operational domain study using SimAnneal in place of ExhaustiveGS as long as simulations are given a long enough runtime to reach a high confidence level. Runtimes can be informed by a past study on the time-to-solution of SiQAD ground state simulators [12].

The acquisition of operational domains remains a computationally-intensive process. Currently available methodologies for finding operational domains work best with gates that exhibit a higher level of symmetry. We, therefore, chose to perform the analysis on the And3 gate. When operational domain analysis techniques become better understood, it will be worthwhile to revisit other designs. The above And3 operational domain analysis serves to provide an example; it will be worthwhile for future work to investigate more efficient methods of acquiring operational domains and the formulation of an associated figure of merit. The raw simulation results are made available in the public repository listed in Section I.

V. Discussions and Future work

This article presented a novel and complete 3-input NPN gate library for atomic silicon quantum dots, a fundamental development that can lead to more compact SiDB circuits than previously achieved in the field. The extraordinary flexibility offered by the SiDB platform enabled this work to propose novel gates that correspond to canonical 3-input NPN class representatives. Combining these advantages with a readily available CAD tool calibrated to experimental results, there exists ample opportunities to conduct further research into SiDB logic as a direction for post-CMOS research.

To take this work forward, we believe that designing a standardized input and output wire library will be a key step towards enabling scalable circuit designs and motivating the development of electronic design automation tools for this novel technology. Lastly, it will be of great interest to develop formal procedures to obtain a figure of merit for the evaluation and comparison of operational domains between different designs.

Acknowledgments

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References

[1] N. G. Anderson and S. Bhanja, *Field-Coupled Nanocomputing*, 1st ed. Springer-Verlag Berlin Heidelberg, 2014.

[2] T. R. Huff, H. Labidi, M. Rashidi, M. Koleini, R. Achal, M. H. Salomons, and R. A. Wolkow, "Atomic white-out: enabling atomic circuitry through mechanically induced bonding of single hydrogen atoms to a silicon surface," *ACS Nano*, vol. 11, no. 9, pp. 8636–8642, Sep. 2017.

[3] R. Achal, M. Rashidi, J. Croshaw, D. Churchill, M. Taucer, T. Huff, M. Cloutier, J. Pitters, and R. A. Wolkow, "Lithography for robust and editable atomic-scale silicon devices and memories," *Nature Communications*, vol. 9, no. 1, p. 2778, Jul. 2018.

[4] T. Huff, H. Labidi, M. Rashidi, L. Livadaru, T. Dienel, R. Achal, W. Vine, J. Pitters, and R. Wolkow, "Binary atomic silicon logic," *Nature Electronics*, vol. 1, p. 636, 12 2018.

[5] S. S. H. Ng, J. Retallick, H. N. Chiu, R. Lupoiu, L. Livadaru, T. Huff, M. Rashidi, W. Vine, T. Dienel, R. A. Wolkow, and K. Walus, "Siqad: A design and simulation tool for atomic silicon quantum dot circuits," *IEEE Transactions on Nanotechnology*, vol. 19, pp. 137–146, 2020.

[6] A. N. Bahar, K. A. Wahid, S. S. Ahmadpour, and M. Mosleh, "Atomic silicon quantum dot: A new designing paradigm of an atomic logic circuit," *IEEE Transactions on Nanotechnology*, vol. 19, 2020.

[7] M. D. Vieira, I. G. S. Moreira, P. A. R. L. Silva, L. O. Luz, R. S. Ferreira, O. P. Vilela Neto, and J. A. M. Nacif, "Novel three-input gates for silicon quantum dot," in *2021 34th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI)*, 2021, pp. 1–6.

[8] D. S. Marakkalage, E. Testa, H. Riener, A. Mishchenko, M. Soeken, and G. De Micheli, "Three-input gates for logic synthesis," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2020.

[9] J. M. Matos, J. Carrabina, and A. Reis, "Efficiently mapping vlsi circuits with simple cells," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 38, no. 4, pp. 692–704, 2019.

[10] L. Amarú, P.-E. Gaillardon, and G. De Micheli, "The EPFL Combinational Benchmark Suite," in *International Workshop on Logic and Synthesis (IWLS)*, 2015.

[11] T. R. Huff, T. Dienel, M. Rashidi, R. Achal, L. Livadaru, J. Croshaw, and R. A. Wolkow, "Electrostatic landscape of a Hydrogen-terminated silicon surface probed by a moveable quantum dot," *ACS Nano*, vol. 13, no. 9, pp. 10 566–10 575, Sep. 2019.

[12] S. S. H. Ng, "Computer-aided design of atomic silicon quantum dots and computational applications," Master's thesis, University of British Columbia, 2020.

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