fiction – An Open Source Framework for the Design of Field-coupled Nanocomputing Circuits

Marcel Walter[1] Robert Wille[2,3] Frank Sill Torres[3]
Daniel Große[1,3] Rolf Drechsler[1,3]

[1] Research Group of Computer Architecture, University of Bremen, Germany
[2] Institute for Integrated Circuits, Johannes Kepler University Linz, Austria
[3] Cyber-Physical Systems, DFKI GmbH, Germany

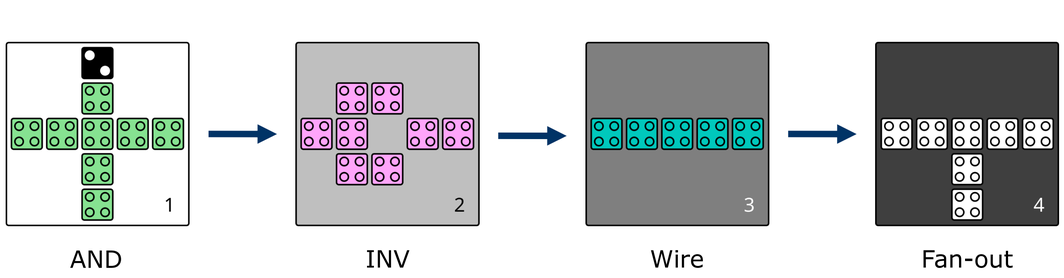
m_walter@uni-bremen.de

Abstract

As a class of emerging post-CMOS technologies, **Field-coupled Nanocomputing (FCN)** [1] promises computation with tremendously low energy dissipation. Even though ground breaking advances in several physical implementations like **Quantum-dot Cellular Automata (QCA)** or **Nanomagnet Logic (NML)** have been made in the last couple of years, design automation for FCN is still in its infancy and often still relies on manual labor. In this work, we present an open source framework called ***fiction*** for physical design and technology mapping of FCN circuits. Its efficient data structures, state-of-the-art algorithms, and extensibility provide a basis for future research in the domain.

FCN Design

- Computations and data transfer is realized via repelling forces on a quantum level between nanoscale **cells arranged in patterned arrays**.
- Data flow is only possible due to shifted and **consecutively numbered external clocks**.
- FCN cells can be grouped in **tiles** controlled by the same external clock and thereby **forming logic elements**.



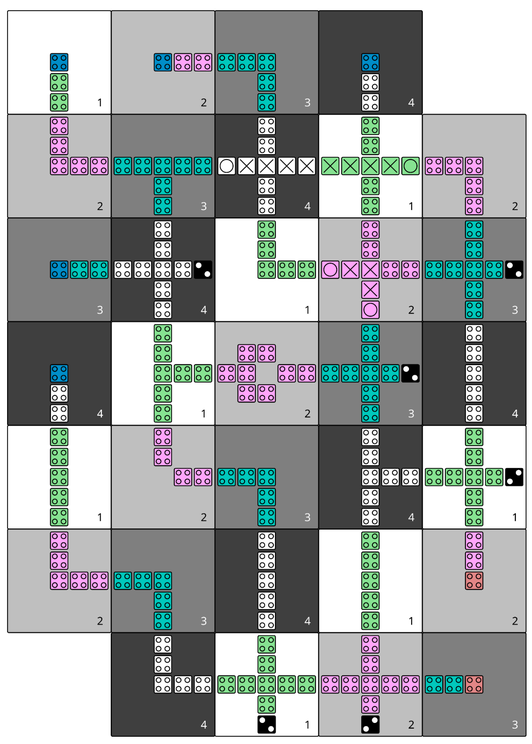
Challenges

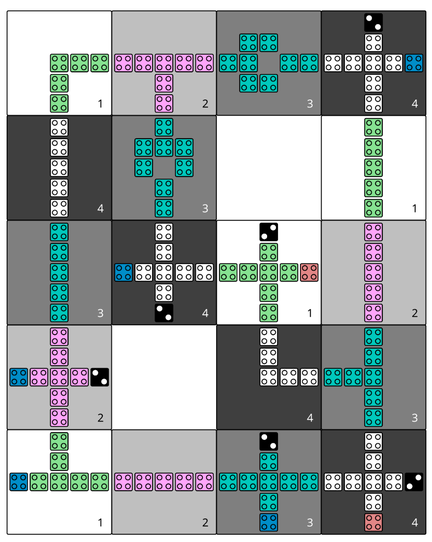
- Wires and gates are **equally expensive**.
- Data flow must be **synchronized** locally and globally.
- Area, delay, and the use of crossings is to be **minimized**.
- Placement, routing, and timing are strongly interdependent.
- Specialized **logic synthesis** is still missing.

Case Study

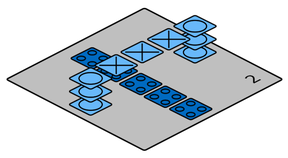
The implemented SMT-based **exact physical design** algorithm [2] allows to explore the design features supported by ***fiction***. Applying various cost metrics, designers can get an intuition for the features' impact on different layouts.

Exemplarily, in the figures shown below, the same *ISCAS85 c17* circuit is presented. On the left, it was optimized for **integration** (accessible I/O pins) and **throughput**. On the right hand side, the design objective was circuit **area**.



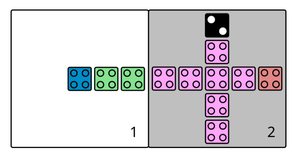


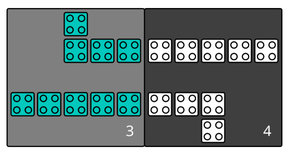
Feature Overview



FCN technologies are often considered to be planar with limited crossing capabilities. Since some layouts (like XOR) cannot be generated crossing-free, ***fiction*** offers support for **multi-layer crossings**.

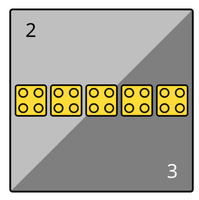
In literature, both can be found: pin cells as part of gate structures and **designated I/O elements** located outside of gates. Both approaches are fully supported and available in all algorithms.





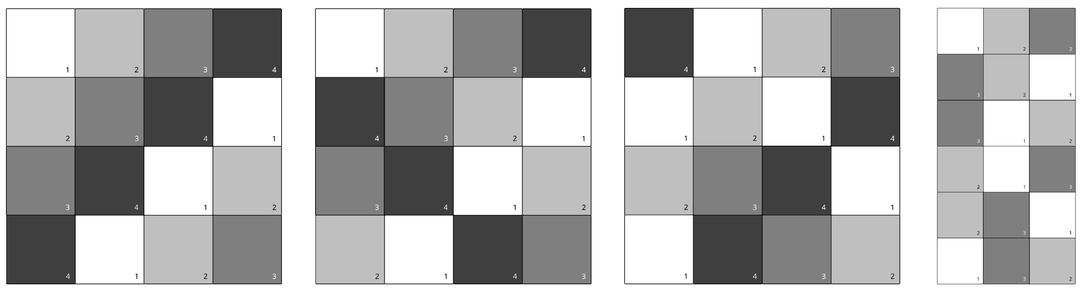
Gate-level abstraction has its limits. Often, chip area is wasted when only using a single wire per tile. In ***fiction***, **multi-wires** are supported allowing for more flexible physical design approaches.

When making smart use of external clocks, artificial **synchronization elements** [3] can be created which stall signals for several clock phases. This cannot only implement latches in an area efficient way, but it can also help overcoming local clock synchronization issues [5]. Synchronization elements for both use cases are fully supported in ***fiction***.



Clocking Schemes

Clocking schemes (floor plans) can help pruning the search space during physical design. Several ones are predefined in ***fiction***, irregular schemes are supported, and custom ones can easily be implemented.



Physical Design Algorithms

Two state-of-the-art physical design algorithms are already implemented in ***fiction***: (1) an **SMT-based exact** approach [2] which allows for exploration of design features shown above and is applicable to rather small circuits; and (2) a non-minimal but **scalable linear-time approximation** [4] that assumes a fixed clocking scheme and handles 2000X larger AIGs than the former s-o-t-a.

Selected Publications

[1] N. G. Anderson and S. Bhanja. Field-coupled Nanocomputing: Paradigms, Progress, and Perspectives. *Springer*, New York (2014).

[2] M. Walter, R. Wille, D. Große, F. S. Torres, and R. Drechsler. An Exact Method for Design Exploration of Quantum-dot Cellular Automata. *DATE* (2018).

[3] F. S. Torres, M. Walter, R. Wille, D. Große, and R. Drechsler. Synchronization of Clocked Field-Coupled Circuits. *IEEE-NANO* (2018).

[4] M. Walter, R. Wille, F. S. Torres, D. Große, and R. Drechsler. Scalable Design for Field-coupled Nanocomputing Circuits. *ASP-DAC* (2019).

[5] R. Wille, M. Walter, F. S. Torres, D. Große, R. Drechsler. Ignore Clocking Constraints: An Alternative Physical Design Methodology for Field-coupled Nanocomputing Circuits. *ISVLSI* (2019).

Scan me!

https://github.com/marcelwa/fiction